



H61H2-M2

Rev : 1.0

ECS CONFIDENTIAL

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23	SIO-IT8758E
24	AUDIO VT1705/ALC662(CHIP)
25	AUDIO VT1705/ALC662(PANEL)

NOTE:

Design by 428971_428971_Sugar_Bay_and_BromolowWS_PDG_Rev_0_8.pdf,
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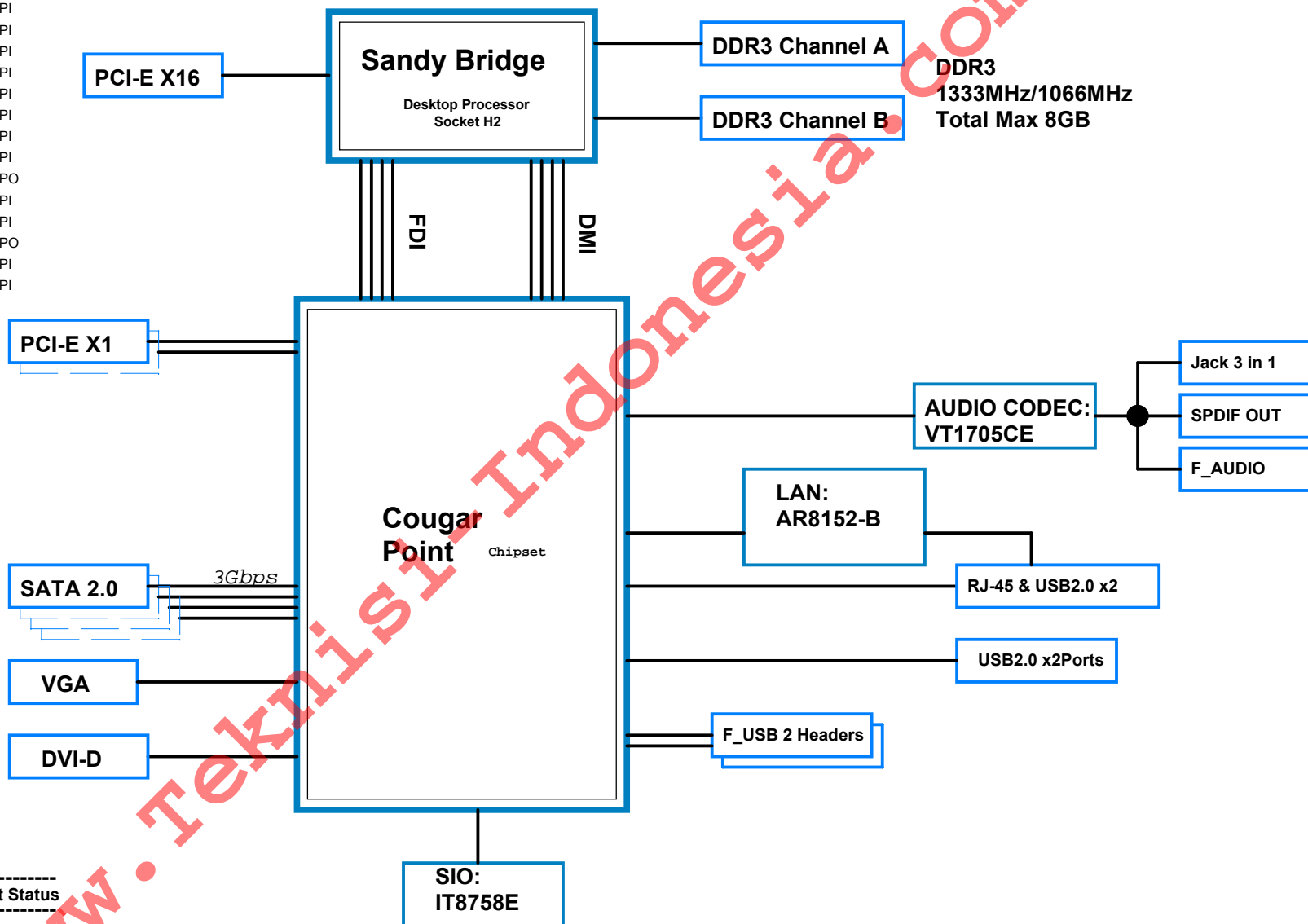
REVISION HISTORY:

Rev	Date	Notes
V.A	2010/09/23	Change from H67H2-M3 1. Audio change to vt1705 2. Super IO change to IT8758E 3. VCore PWM change to RT8859M 4. V_CPUVTT PWM change to RT8121 5. LAN change to AR8151-B & AR8152-B 6. Del PCI function 7. Del USB3.0 function 8. Del SATA 6G 9. Del Easy Charge Circuit of F_USB1
V.1.0	2010/12/03	1. PSON- Pull High 從5VSB改為3VSB_IO 2. Del EC33 1000U-6.3DL-O 3. Change EC35 from (1000U-6.3DL) to (820U-2.5D6-OS) 4. Del EC24 100U-16DE-O 5. 更改DDR3 SOCKET 顏色為兩根都灰色 6. 更改BATTERY SOCKET換成非架高料 7. 更改POWER CONN. 24pin 換成半透明STD料 8. 更改F_USB1改成和F_USB2為相同的顏色 9. VT1705更改為VT1705CE 10. SATA0GP、SATA1GP、SATA2GP、SATA3GP、SATA4GP、SATA5GP 增加Pull High & Low線路

 Elitegroup Computer Systems		
Title		
Cover Page		
Size	Document Number	Rev
Custom	H61H2-M2	1.0
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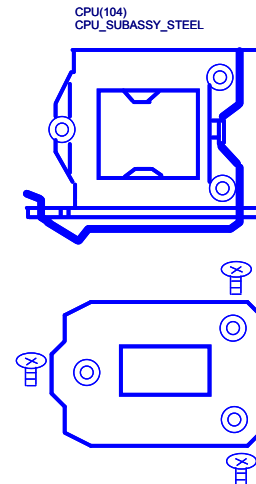
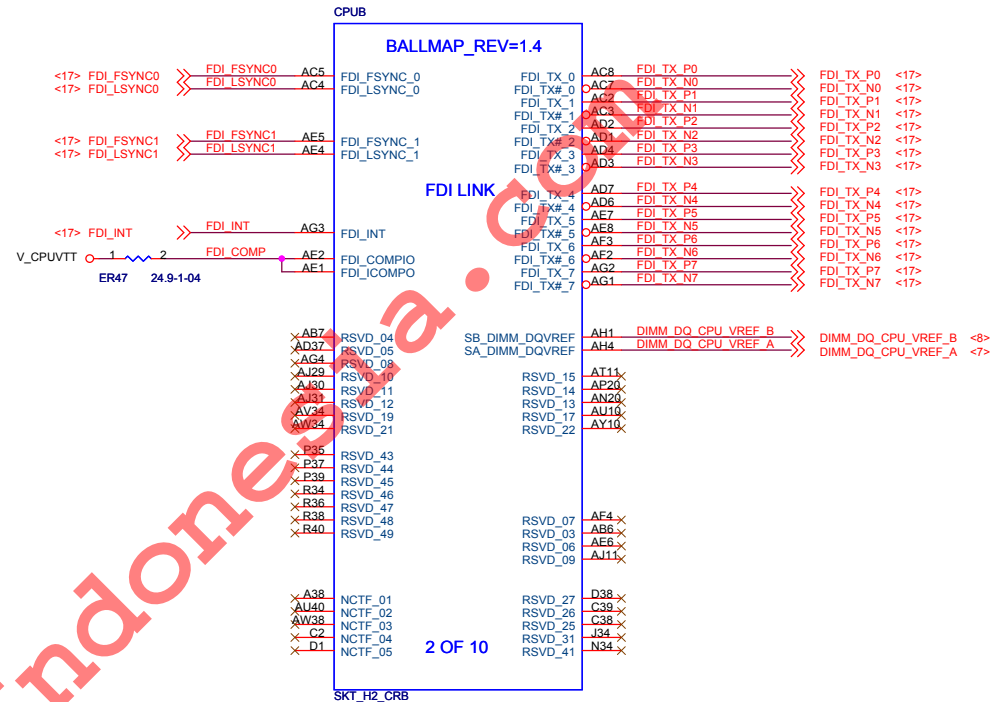
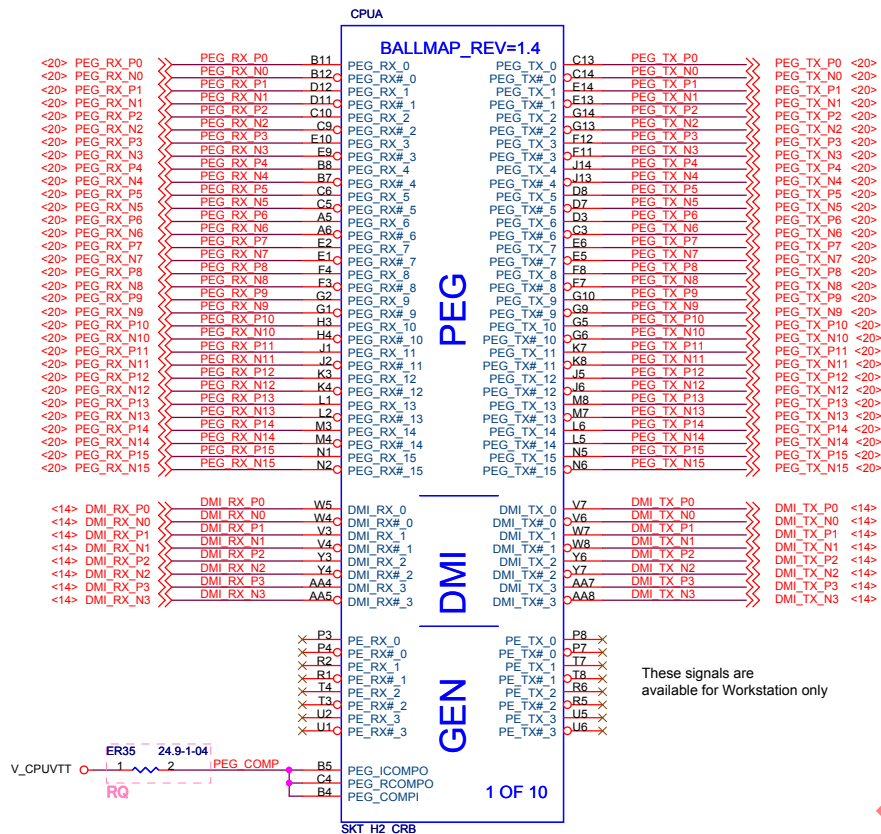
PCH-GPIO function

Pin Name	Power Well	Usage	Default Status
GPIO71	VCC3		GPI
GPIO22	VCC3		GPI
GPIO38	VCC3		GPI
GPIO39	VCC3		GPI
GPIO48	VCC3		GPI
GPIO21	VCC3		GPI
GPIO36	VCC3		GPI
GPIO37	VCC3		GPI
GPIO16	VCC3	Reserve for TPM	GPI
GPIO49	VCC3	Reserve for TPM	GPI
GPIO00	VCC3	F_AUDIO Detect	GPI
GPIO33	VCC3	ME Enable/Disable	GPO
GPIO34	VCC3	pull-up	GPI
GPIO13	3VSB	PME	GPI
GPIO24	3VSB	SKTOCC	GPO
GPIO57	3VSB	Board ID(CRB_0.7)	GPI
GPIO61	3VSB	TPM_LPCPD	GPI



SIO-GPIO function

Pin Name	Power Well	Usage	Default Status
GP16	VCC3	BEEP	
GP23		Power LED	
GP22		Power LED	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	
Pin Name		Usage	



01D201-000060 PCH E60

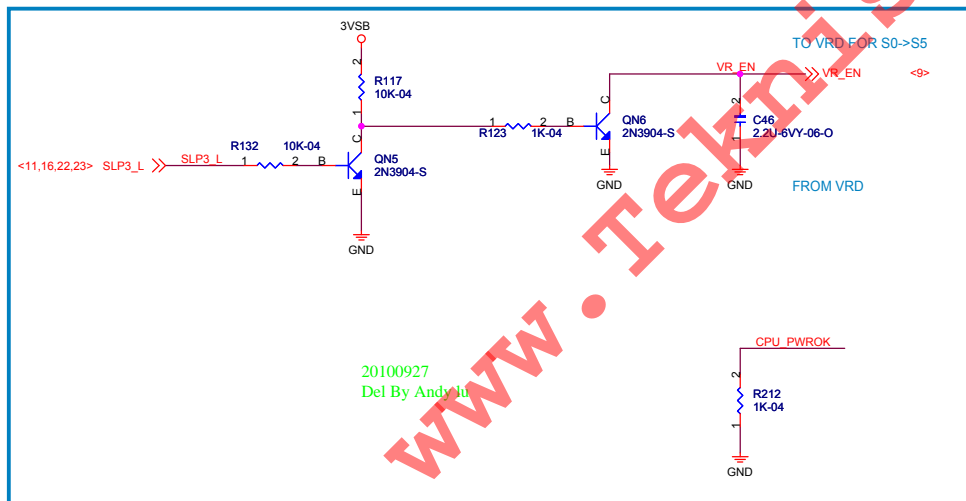
CFG	H	L	DESCRIPTION
0	reserved	reserved	reserved
1	reserved	reserved	reserved
2	NORMAL	REVERSE	PEGLANE REVERSAL[0], X16
3	reserved	reserved	reserved
4	reserved	reserved	reserved
5	*	*	PEOFSEL[0]
6	*	*	PEOFSEL[1]
7	reserved	reserved	reserved
8	reserved	reserved	reserved
9	reserved	reserved	reserved
10	reserved	reserved	reserved
11	reserved	reserved	reserved
12	reserved	reserved	reserved
13	reserved	reserved	reserved
14	reserved	reserved	reserved
15	reserved	reserved	reserved

CFG[0..17] HAVE INTERNAL PULL-UPS

PCIE CONFIG	SELO	SEL1
1 X 16	1	1
2 X 8	0	1

CFG[5:6]:
 01=DEFAULT X16,
 01=X28,
 10=RESERVED,
 00=X8,X4,X4

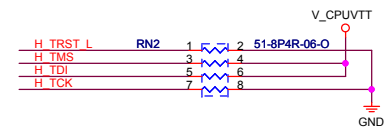
Power Down Sequencing Circuit



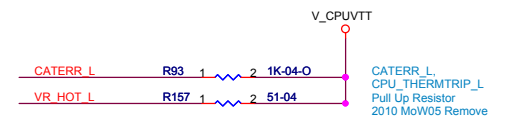
change test point for internal PU Jack05/25

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SKT_H2_CRB



EDS P68/132 has internal PU Jack05/25



DMI/FDI termination voltage:
 DC coupled: TX/RX to VCC ISF sampled high
 DC coupled: TX/RX to VSS IF sampled low
 AC COUPLED: TX set to VCC/2, RX set to VSS regardless of this strap

<7> M_DATA_A[0..63]	<<> M_DATA_A[0..63]
<7> M_DQS_A_P[0..7]	<<> M_DQS_A_P[0..7]
<7> M_DQS_A_N[0..7]	<<> M_DQS_A_N[0..7]
<7> M_MA_A[0..15]	<<> M_MA_A[0..15]
<7> M_BS_A[0..2]	<<> M_BS_A[0..2]
<7> M_CS_A_L[0..1]	<<> M_CS_A_L[0..1]
<7> M_CKE_A[0..1]	<<> M_CKE_A[0..1]
<7> M_ODT_A[0..1]	<<> M_ODT_A[0..1]
<7> M_CLK_A_P[0..1]	<<> M_CLK_A_P[0..1]
<7> M_CLK_A_N[0..1]	<<> M_CLK_A_N[0..1]
<7> M_WE_A_L	<<> M_WE_A_L
<7> M_CAS_A_L	<<> M_CAS_A_L
<7> M_RAS_A_L	<<> M_RAS_A_L

DDR3 CH.A

<7,8> DDR3_DRAMRST_L <<> DDR3_DRAMRST_L

<8> M_DATA_B[0..63]	<<> M_DATA_B[0..63]
<8> M_DQS_B_P[0..7]	<<> M_DQS_B_P[0..7]
<8> M_DQS_B_N[0..7]	<<> M_DQS_B_N[0..7]
<8> M_MA_B[0..15]	<<> M_MA_B[0..15]
<8> M_BS_B[0..2]	<<> M_BS_B[0..2]
<8> M_CS_B_L[0..1]	<<> M_CS_B_L[0..1]
<8> M_CKE_B[0..1]	<<> M_CKE_B[0..1]
<8> M_ODT_B[0..1]	<<> M_ODT_B[0..1]
<8> M_CLK_B_P[0..1]	<<> M_CLK_B_P[0..1]
<8> M_CLK_B_N[0..1]	<<> M_CLK_B_N[0..1]
<8> M_WE_B_L	<<> M_WE_B_L
<8> M_CAS_B_L	<<> M_CAS_B_L
<8> M_RAS_B_L	<<> M_RAS_B_L

DDR3 CH.B

M_DATA_A0	AJ3	SA_DQ_0	SA_MA_0	AV27	M_MA_A0
M_DATA_A1	AJ4	SA_DQ_1	SA_MA_1	AV24	M_MA_A1
M_DATA_A2	AL3	SA_DQ_2	SA_MA_2	AW24	M_MA_A2
M_DATA_A3	AL4	SA_DQ_3	SA_MA_3	AW23	M_MA_A3
M_DATA_A4	AJ2	SA_DQ_4	SA_MA_4	AV23	M_MA_A4
M_DATA_A5	AJ1	SA_DQ_5	SA_MA_5	AT24	M_MA_A5
M_DATA_A6	AL2	SA_DQ_6	SA_MA_6	AT23	M_MA_A6
M_DATA_A7	AL1	SA_DQ_7	SA_MA_7	AV22	M_MA_A7
M_DATA_A8	AN1	SA_DQ_8	SA_MA_8	AT22	M_MA_A8
M_DATA_A9	AR3	SA_DQ_9	SA_MA_9	AV28	M_MA_A10
M_DATA_A10	AR4	SA_DQ_10	SA_MA_10	AV21	M_MA_A11
M_DATA_A11	AN2	SA_DQ_11	SA_MA_11	AT21	M_MA_A12
M_DATA_A12	AN3	SA_DQ_12	SA_MA_12	AW32	M_MA_A13
M_DATA_A13	AR2	SA_DQ_13	SA_MA_13	AU20	M_MA_A14
M_DATA_A14	AR1	SA_DQ_14	SA_MA_14	AT20	M_MA_A15
M_DATA_A15	AV2	SA_DQ_15	SA_MA_15		
M_DATA_A16	AW3	SA_DQ_16			
M_DATA_A17	AW5	SA_DQ_17			
M_DATA_A18	AW5	SA_DQ_18	SA_WE#	AW29	M_WE_A_L
M_DATA_A19	AU2	SA_DQ_19	SA_CAS#	AV30	M_CAS_A_L
M_DATA_A20	AU2	SA_DQ_20	SA_RAS#	AU28	M_RAS_A_L
M_DATA_A21	AU5	SA_DQ_21			
M_DATA_A22	AY5	SA_DQ_22			
M_DATA_A23	AY7	SA_DQ_23	SA_BS_0	AY29	M_BS_A0
M_DATA_A24	AU7	SA_DQ_24	SA_BS_1	AW24	M_BS_A1
M_DATA_A25	AV9	SA_DQ_25	SA_BS_2	AV20	M_BS_A2
M_DATA_A26	AV9	SA_DQ_26			
M_DATA_A27	AV7	SA_DQ_27			
M_DATA_A28	AW7	SA_DQ_28	SA_CS#_0	AU29	
M_DATA_A29	AW7	SA_DQ_29	SA_CS#_1	AV32	
M_DATA_A30	AW9	SA_DQ_30	SA_CS#_2	AW30	M_CS_A_L0
M_DATA_A31	AJ3	SA_DQ_31	SA_CS#_3	AU33	M_CS_A_L1
M_DATA_A32	AJ3	SA_DQ_32			
M_DATA_A33	AW37	SA_DQ_33			
M_DATA_A34	AJ3	SA_DQ_34			
M_DATA_A35	AJ3	SA_DQ_35	SA_CKE_0	AV19	
M_DATA_A36	AW35	SA_DQ_36	SA_CKE_1	AT19	
M_DATA_A37	AW38	SA_DQ_37	SA_CKE_2	AU18	M_CKE_A0
M_DATA_A38	AJ3	SA_DQ_38	SA_CKE_3	AV18	M_CKE_A1
M_DATA_A39	AJ3	SA_DQ_39			
M_DATA_A40	AR40	SA_DQ_40			
M_DATA_A41	AR37	SA_DQ_41			
M_DATA_A42	AN38	SA_DQ_42	SA_ODT_0	AV31	
M_DATA_A43	AN37	SA_DQ_43	SA_ODT_1	AJ32	
M_DATA_A44	AR39	SA_DQ_44	SA_ODT_2	AU30	M_ODT_A0
M_DATA_A45	AR38	SA_DQ_45	SA_ODT_3	AW33	M_ODT_A1
M_DATA_A46	AN39	SA_DQ_46			
M_DATA_A47	AN40	SA_DQ_47			
M_DATA_A48	AL37	SA_DQ_48			
M_DATA_A49	AL38	SA_DQ_49	SA_CK_0	AY25	
M_DATA_A50	AJ38	SA_DQ_50	SA_CK#_0	AW25	
M_DATA_A51	AJ37	SA_DQ_51	SA_CK_1	AU24	
M_DATA_A52	AL39	SA_DQ_52	SA_CK#_1	AU25	
M_DATA_A53	AL38	SA_DQ_53	SA_CK_2	AW27	M_CLK_A_P0
M_DATA_A54	AJ39	SA_DQ_54	SA_CK#_2	AY27	M_CLK_A_N0
M_DATA_A55	AJ40	SA_DQ_55	SA_CK_3	AW26	M_CLK_A_P1
M_DATA_A56	AG40	SA_DQ_56	SA_CK#_3	AW26	M_CLK_A_N1
M_DATA_A57	AG37	SA_DQ_57			
M_DATA_A58	AE38	SA_DQ_58			
M_DATA_A59	AE37	SA_DQ_59			
M_DATA_A60	AG38	SA_DQ_60	SM_DRAMRST#	AW18	DDR3_DRAMRST_L
M_DATA_A61	AE38	SA_DQ_61			
M_DATA_A62	AE39	SA_DQ_62	SA_DQS_8	AV13	
M_DATA_A63	AE40	SA_DQ_63	SA_DQS_8	AV14	
M_DQS_A_P0	AK3	SA_DQS_0			
M_DQS_A_P1	AP3	SA_DQS_1			
M_DQS_A_P2	AW4	SA_DQS_2			
M_DQS_A_P3	AV8	SA_DQS_3			
M_DQS_A_P4	AP37	SA_DQS_4	SA_ECC_CB_0	AU12	
M_DQS_A_P5	AP38	SA_DQS_5	SA_ECC_CB_1	AU14	
M_DQS_A_P6	AK38	SA_DQS_6	SA_ECC_CB_2	AW13	
M_DQS_A_P7	AF38	SA_DQS_7	SA_ECC_CB_3	AY13	
			SA_ECC_CB_4	AU14	
			SA_ECC_CB_5	AU11	
			SA_ECC_CB_6	AY12	
			SA_ECC_CB_7	AW12	
M_DQS_A_N0	AK2	SA_DQS#_0			
M_DQS_A_N1	AP2	SA_DQS#_1			
M_DQS_A_N2	AV4	SA_DQS#_2			
M_DQS_A_N3	AW5	SA_DQS#_3			
M_DQS_A_N4	AV36	SA_DQS#_4			
M_DQS_A_N5	AP39	SA_DQS#_5			
M_DQS_A_N6	AK39	SA_DQS#_6			
M_DQS_A_N7	AF39	SA_DQS#_7			

DDR_0

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SKT_H2_CRB

DDR3 CH.A

Pay Attention to This Part!

M_DATA_B0	AG7	SB_DQ_0	SB_MA_0	AK24	M_MA_B0
M_DATA_B1	AG8	SB_DQ_1	SB_MA_1	AM20	M_MA_B1
M_DATA_B2	AJ9	SB_DQ_2	SB_MA_2	AM19	M_MA_B2
M_DATA_B3	AG6	SB_DQ_3	SB_MA_3	AK18	M_MA_B3
M_DATA_B4	AG6	SB_DQ_4	SB_MA_4	AP19	M_MA_B4
M_DATA_B5	AG6	SB_DQ_5	SB_MA_5	AP18	M_MA_B5
M_DATA_B6	AJ6	SB_DQ_6	SB_MA_6	AM18	M_MA_B6
M_DATA_B7	AJ7	SB_DQ_7	SB_MA_7	AL18	M_MA_B7
M_DATA_B13	AL7	SB_DQ_8	SB_MA_8	AN18	M_MA_B8
M_DATA_B9	AM7	SB_DQ_9	SB_MA_9	AY17	M_MA_B9
M_DATA_B11	AM10	SB_DQ_10	SB_MA_10	AN23	M_MA_B10
M_DATA_B15	AL10	SB_DQ_11	SB_MA_11	AU17	M_MA_B11
M_DATA_B12	AL6	SB_DQ_12	SB_MA_12	AT18	M_MA_B12
M_DATA_B8	AM6	SB_DQ_13	SB_MA_13	AR26	M_MA_B13
M_DATA_B14	AL9	SB_DQ_14	SB_MA_14	AY16	M_MA_B14
M_DATA_B10	AM9	SB_DQ_15	SB_MA_15	AV16	M_MA_B15
M_DATA_B16	AP7	SB_DQ_16			
M_DATA_B17	AR7	SB_DQ_17			
M_DATA_B18	AP10	SB_DQ_18	SA_CK[2]	AR25	M_WE_B_L
M_DATA_B19	AR10	SB_DQ_19	SA_CK[1]	AK25	M_CAS_B_L
M_DATA_B20	AR10	SB_DQ_20	SA_ODT[2]	AP24	M_RAS_B_L
M_DATA_B21	AF6	SB_DQ_21			
M_DATA_B22	AP9	SB_DQ_22			
M_DATA_B23	AR9	SB_DQ_23	SB_BS_0	AP23	M_BS_B0
M_DATA_B24	AM12	SB_DQ_24	SB_BS_1	AM24	M_BS_B1
M_DATA_B25	AM13	SB_DQ_25	SB_BS_2	AW17	M_BS_B2
M_DATA_B26	AR13	SB_DQ_26			
M_DATA_B27	AP13	SB_DQ_27			
M_DATA_B28	AL12	SB_DQ_28	SB_CS#_0	AN25	
M_DATA_B29	AL13	SB_DQ_29	SB_CS#_1	AN26	
M_DATA_B30	AR12	SB_DQ_30	SB_CS#_2	AT25	M_CS_B_L0
M_DATA_B31	AR12	SB_DQ_31	SB_CS#_3	AT26	M_CS_B_L1
M_DATA_B32	AR28	SB_DQ_32			
M_DATA_B33	AR29	SB_DQ_33			
M_DATA_B34	AL28	SB_DQ_34			
M_DATA_B35	AL29	SB_DQ_35	SB_CKE_0	AU16	
M_DATA_B36	AP28	SB_DQ_36	SB_CKE_1	AY15	
M_DATA_B37	AP29	SB_DQ_37	SB_CKE_2	AW15	M_CKE_B0
M_DATA_B38	AM28	SB_DQ_38	SB_CKE_3	AV15	M_CKE_B1
M_DATA_B39	AM29	SB_DQ_39			
M_DATA_B40	AP32	SB_DQ_40			
M_DATA_B41	AP31	SB_DQ_41			
M_DATA_B42	AP35	SB_DQ_42	SB_ODT_0	AL26	
M_DATA_B43	AP34	SB_DQ_43	SB_ODT_1	AP26	
M_DATA_B44	AR32	SB_DQ_44	SB_ODT_2	AM26	M_ODT_B0
M_DATA_B45	AR31	SB_DQ_45	SB_ODT_3	AK26	M_ODT_B1
M_DATA_B46	AR35	SB_DQ_46			
M_DATA_B47	AR34	SB_DQ_47			
M_DATA_B48	AM32	SB_DQ_48			
M_DATA_B52	AM31	SB_DQ_49	SB_CK_0	AL21	
M_DATA_B55	AL35	SB_DQ_50	SB_CK#_0	AL22	
M_DATA_B51	AL32	SB_DQ_51	SB_CK_1	AL20	
M_DATA_B54	AM34	SB_DQ_52	SB_CK#_1	AK20	
M_DATA_B49	AL31	SB_DQ_53	SB_CK#_2	AL23	M_CLK_B_P0
M_DATA_B53	AM35	SB_DQ_54	SB_CK#_2	AM22	M_CLK_B_N0
M_DATA_B50	AL34	SB_DQ_55	SB_CK_2	AP21	M_CLK_B_P1
M_DATA_B56	AH35	SB_DQ_56	SB_CK_3	AN21	M_CLK_B_N1
M_DATA_B57	AH34	SB_DQ_57			
M_DATA_B58	AE34	SB_DQ_58			
M_DATA_B59	AE35	SB_DQ_59			
M_DATA_B60	AJ34	SB_DQ_60			
M_DATA_B62	AF33	SB_DQ_61			
M_DATA_B63	AF35	SB_DQ_62			
		SB_DQ_63			
M_DQS_B_P0	AH7	SB_DQS_0	SB_DQS_8	AN16	
M_DQS_B_P1	AM8	SB_DQS_1	SB_DQS#_8	AN15	
M_DQS_B_P2	AR8	SB_DQS_2			
M_DQS_B_P3	AN13	SB_DQS_3			
M_DQS_B_P4	AP29	SB_DQS_4	SB_ECC_CB_0	AL16	
M_DQS_B_P5	AP33	SB_DQS_5	SB_ECC_CB_1	AP16	
M_DQS_B_P6	AL33	SB_DQS_6	SB_ECC_CB_2	AR16	
M_DQS_B_P7	AG35	SB_DQS_7	SB_ECC_CB_3	AL15	
			SB_ECC_CB_4	AM15	
M_DQS_B_N0	AH6	SB_DQS#_0	SB_ECC_CB_5	AR15	
M_DQS_B_N1	AL8	SB_DQS#_1			
M_DQS_B_N2	AP8	SB_DQS#_2			
M_DQS_B_N3	AN12	SB_DQS#_3			
M_DQS_B_N4	AN28	SB_DQS#_4			
M_DQS_B_N5	AR33	SB_DQS#_5			
M_DQS_B_N6	AM33	SB_DQS#_6			
M_DQS_B_N7	AG34	SB_DQS#_7			

DDR_1

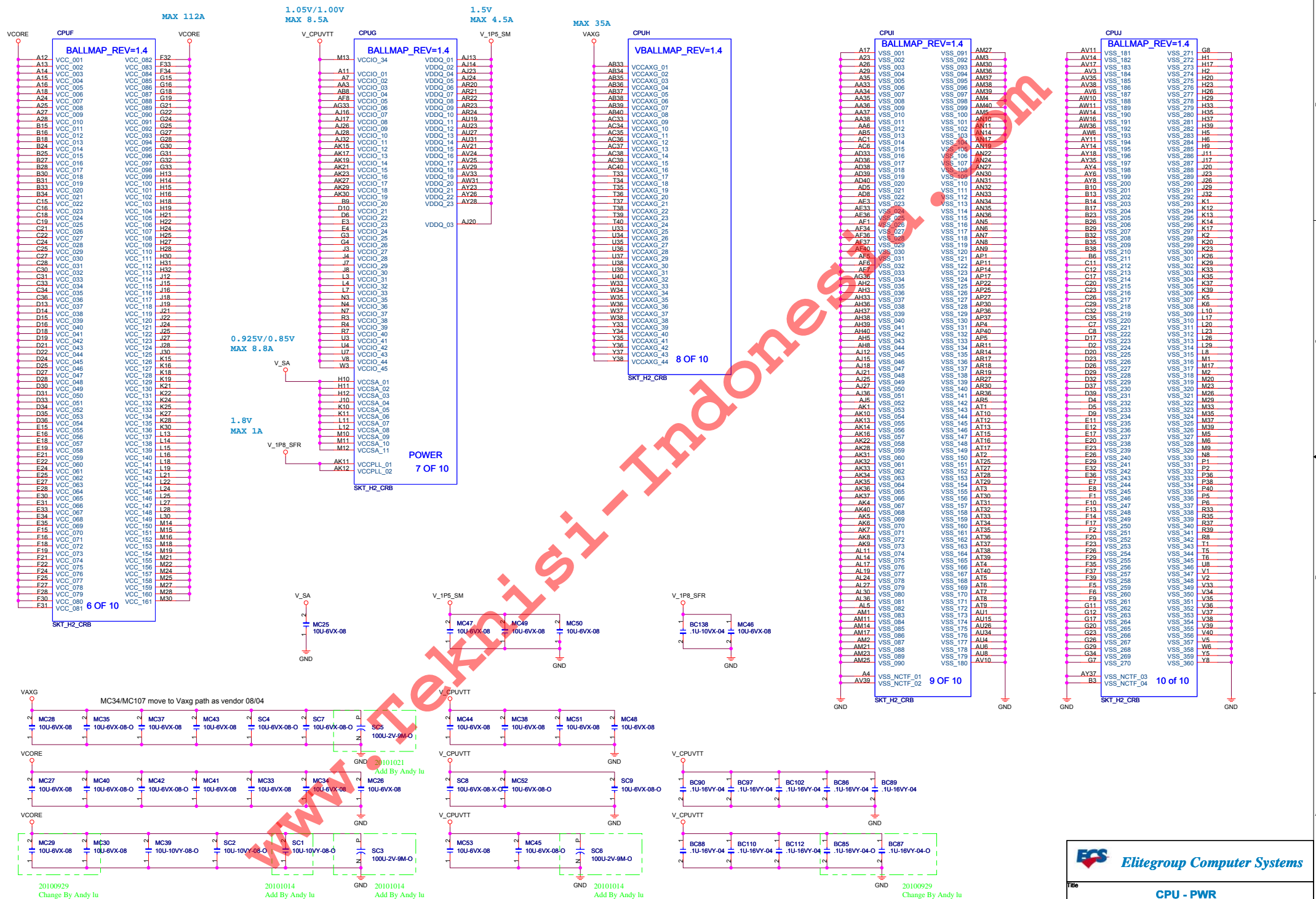
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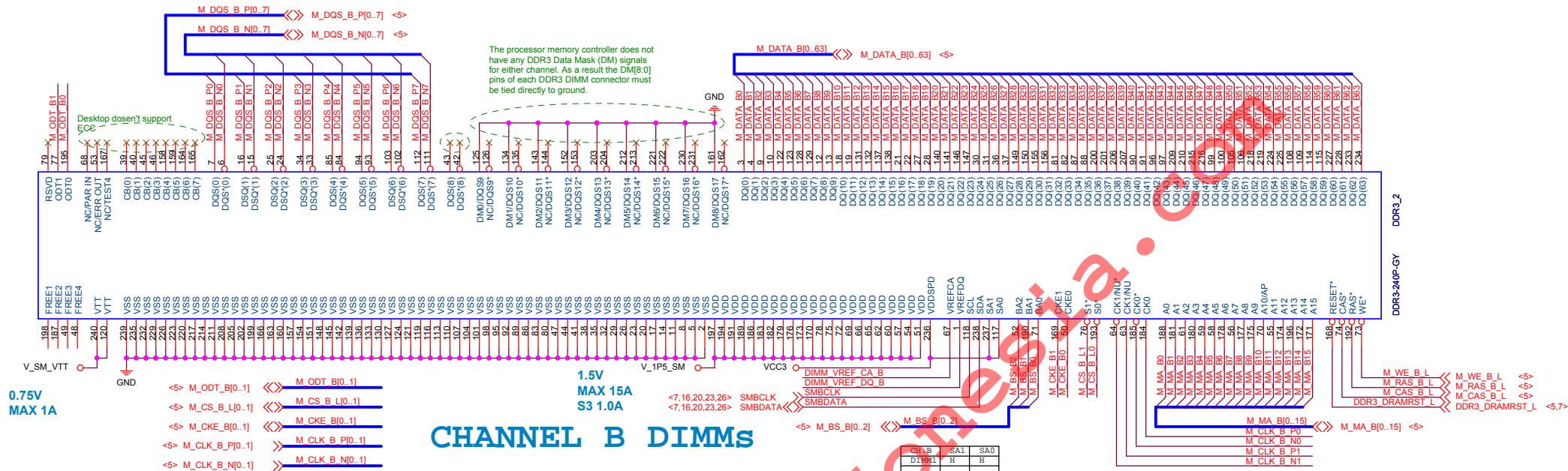
SKT_H2_CRB

DDR3 CH.B

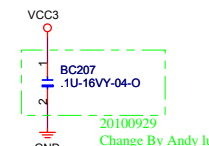
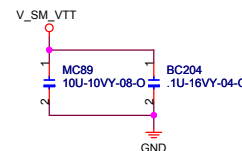
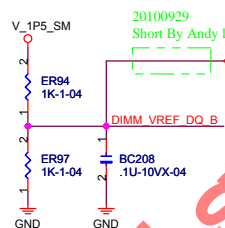
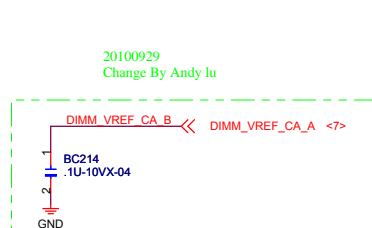
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Title	CPU - DDR3	Rev	1.0
Size Custom	Document Number	H61H2-M2	
Date	Monday, December 06, 2010	Sheet	5 of 29



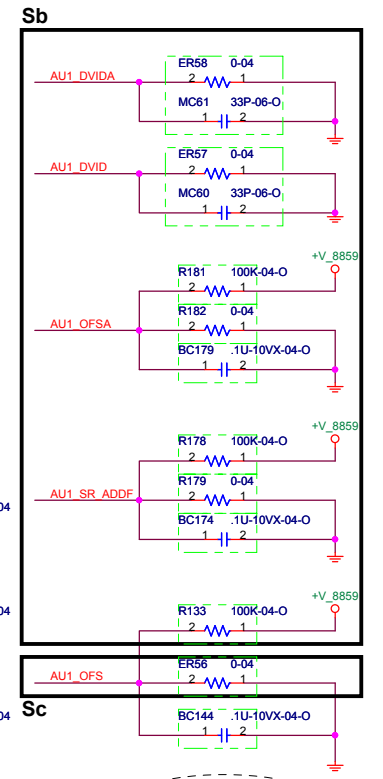
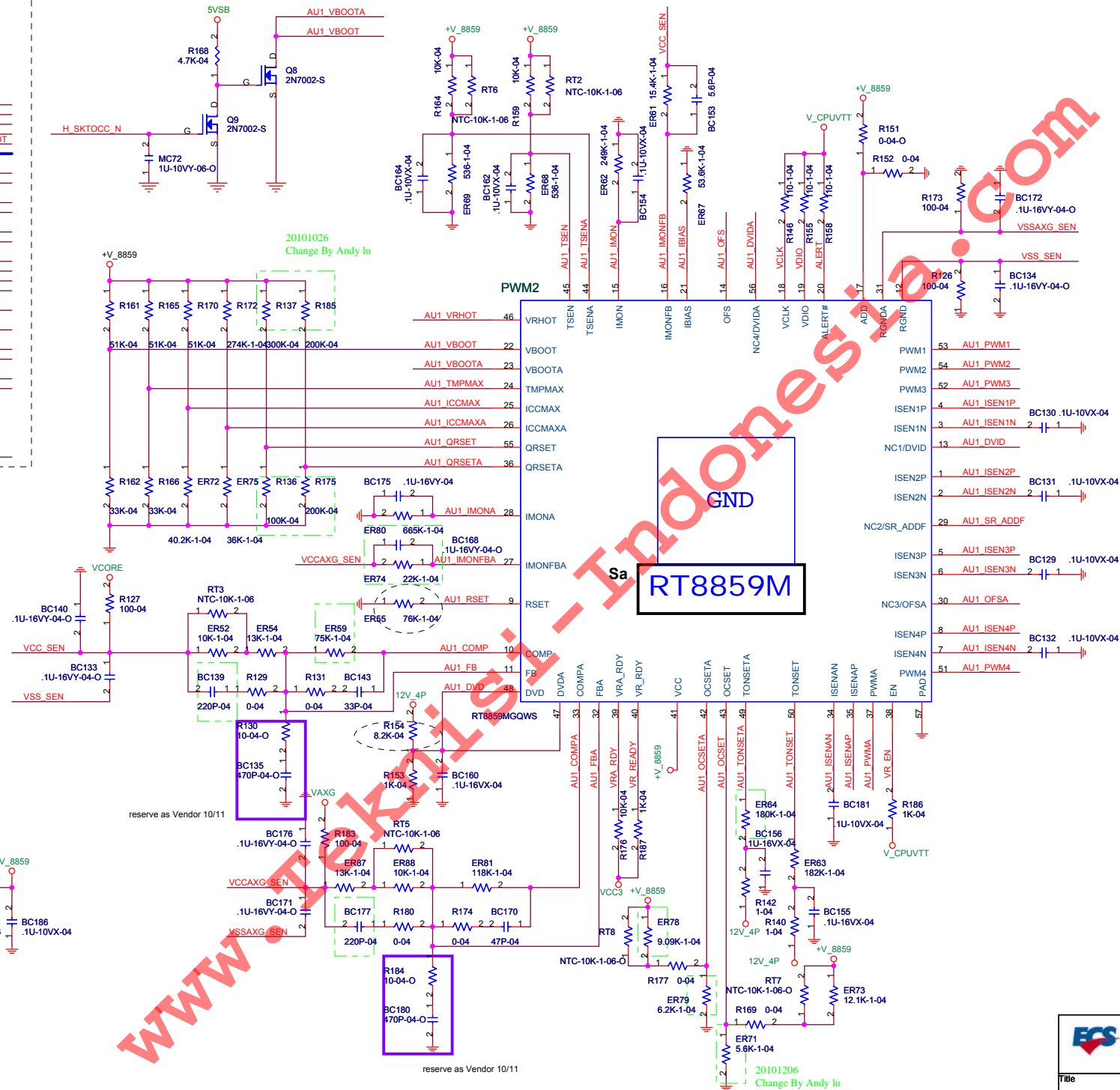
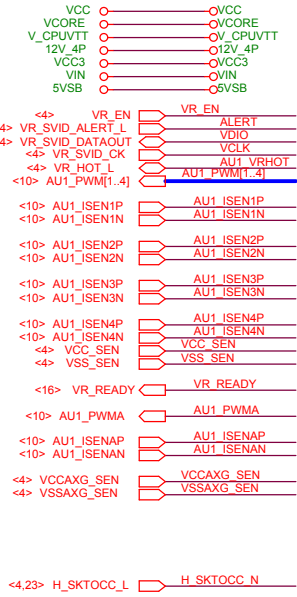


CHANNEL B DIMMs



Del DIMM3 for always populate DIMM4 first Jack 05/13

External Connection



	RT8859A	RT8859M
Sa	RT8859A	RT8859M
Sb	X	V
Sc	402-1-04	1K-1-04

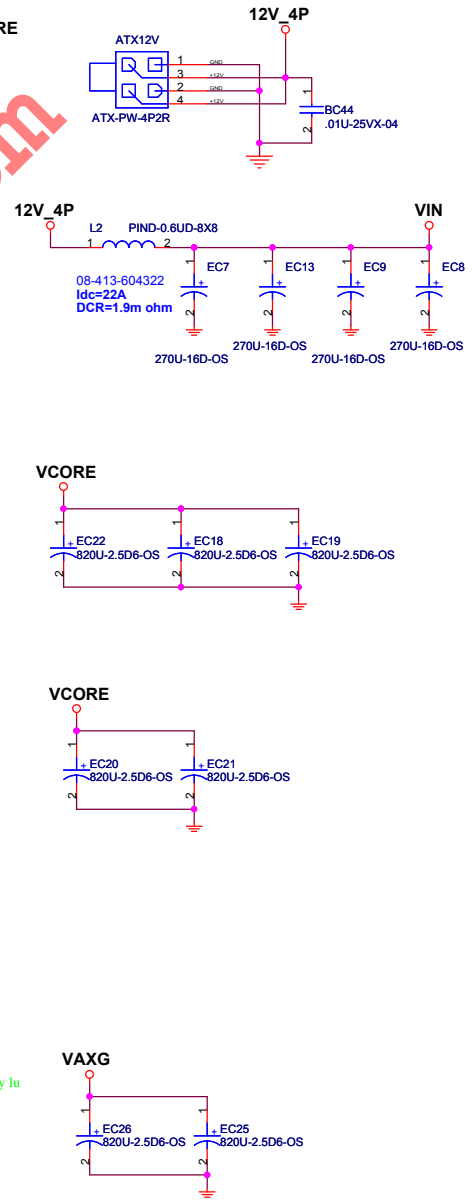
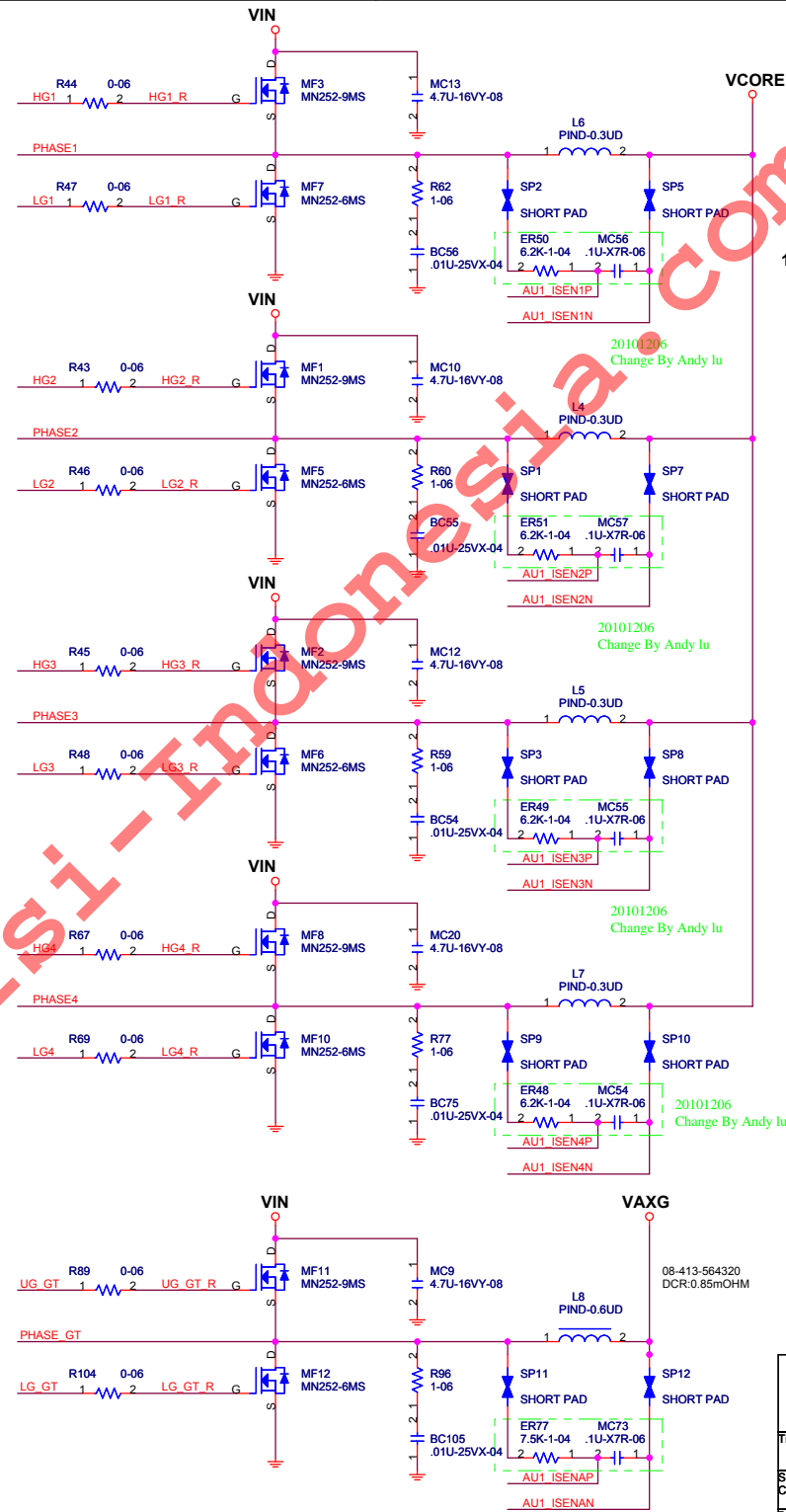
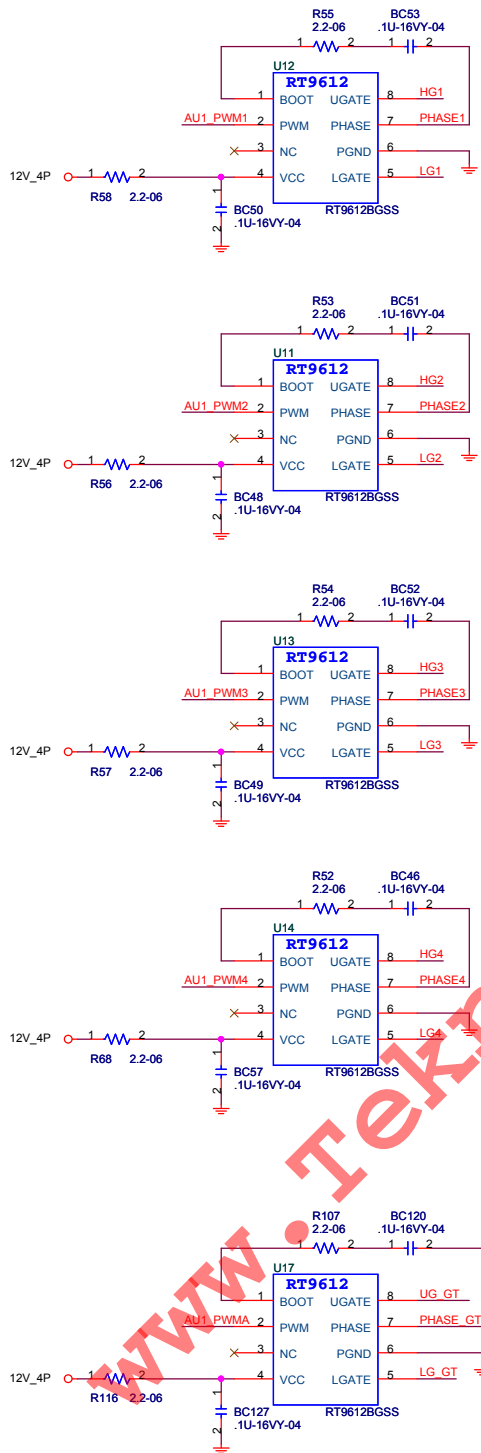
change 1K for OV

External Connection

VCC ○ VCC
V CORE ○ V CORE
12V_4P ○ 12V_4P
VCC3 ○ VCC3
VIN ○ VIN
VAXG ○ VAXG

<9> AU1_PWM[1..4] ○ AU1_PWM[1..4]
<9> AU1_ISEN1P ○ AU1_ISEN1P
<9> AU1_ISEN1N ○ AU1_ISEN1N
<9> AU1_ISEN2P ○ AU1_ISEN2P
<9> AU1_ISEN2N ○ AU1_ISEN2N
<9> AU1_ISEN3P ○ AU1_ISEN3P
<9> AU1_ISEN3N ○ AU1_ISEN3N
<9> AU1_ISEN4P ○ AU1_ISEN4P
<9> AU1_ISEN4N ○ AU1_ISEN4N

<9> AU1_PWMA ○ AU1_PWMA
<9> AU1_ISENAP ○ AU1_ISENAP
<9> AU1_ISENAN ○ AU1_ISENAN

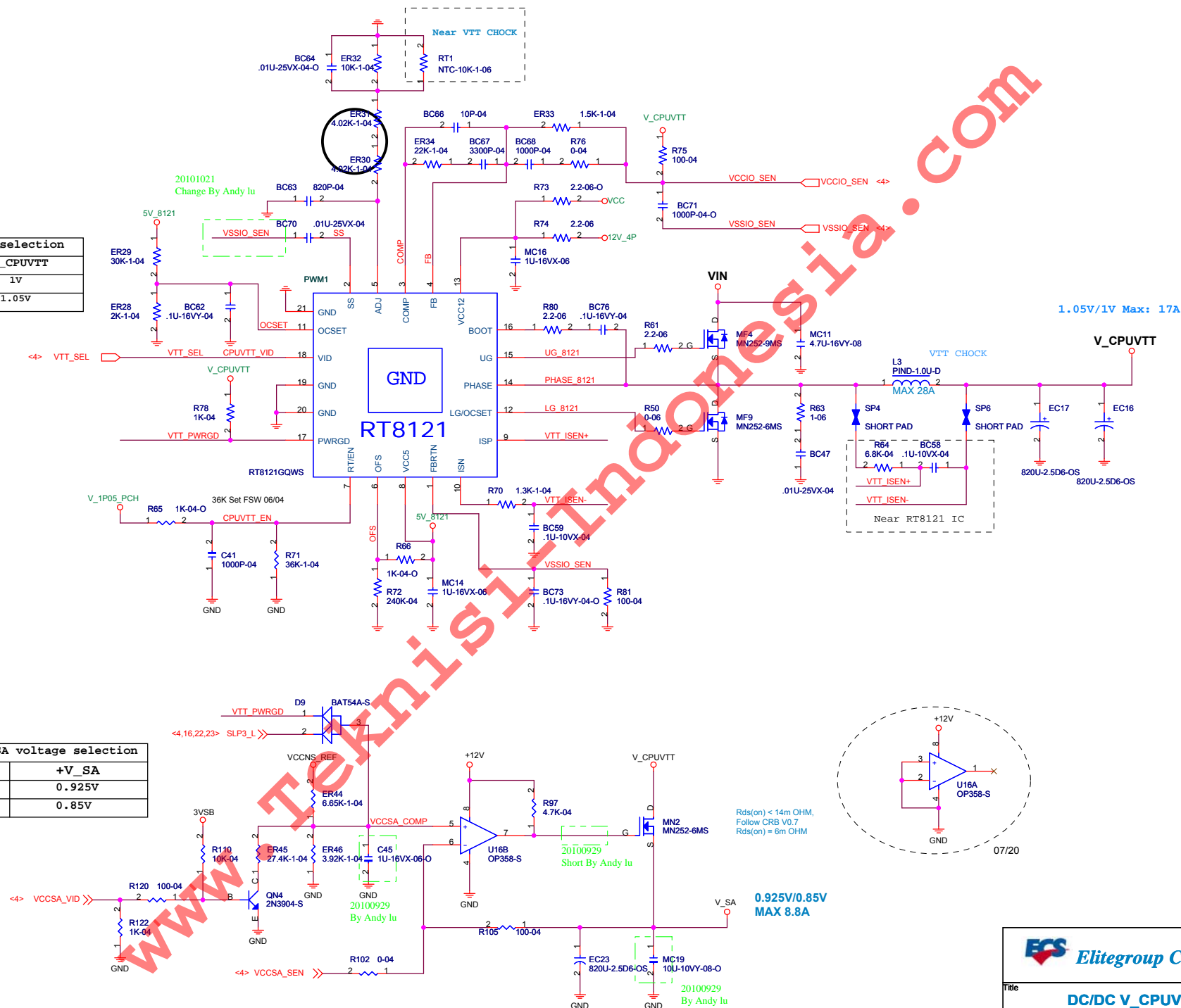


A pin-to-pin connection diagram showing four horizontal lines with circular terminals at both ends. The connections are as follows:

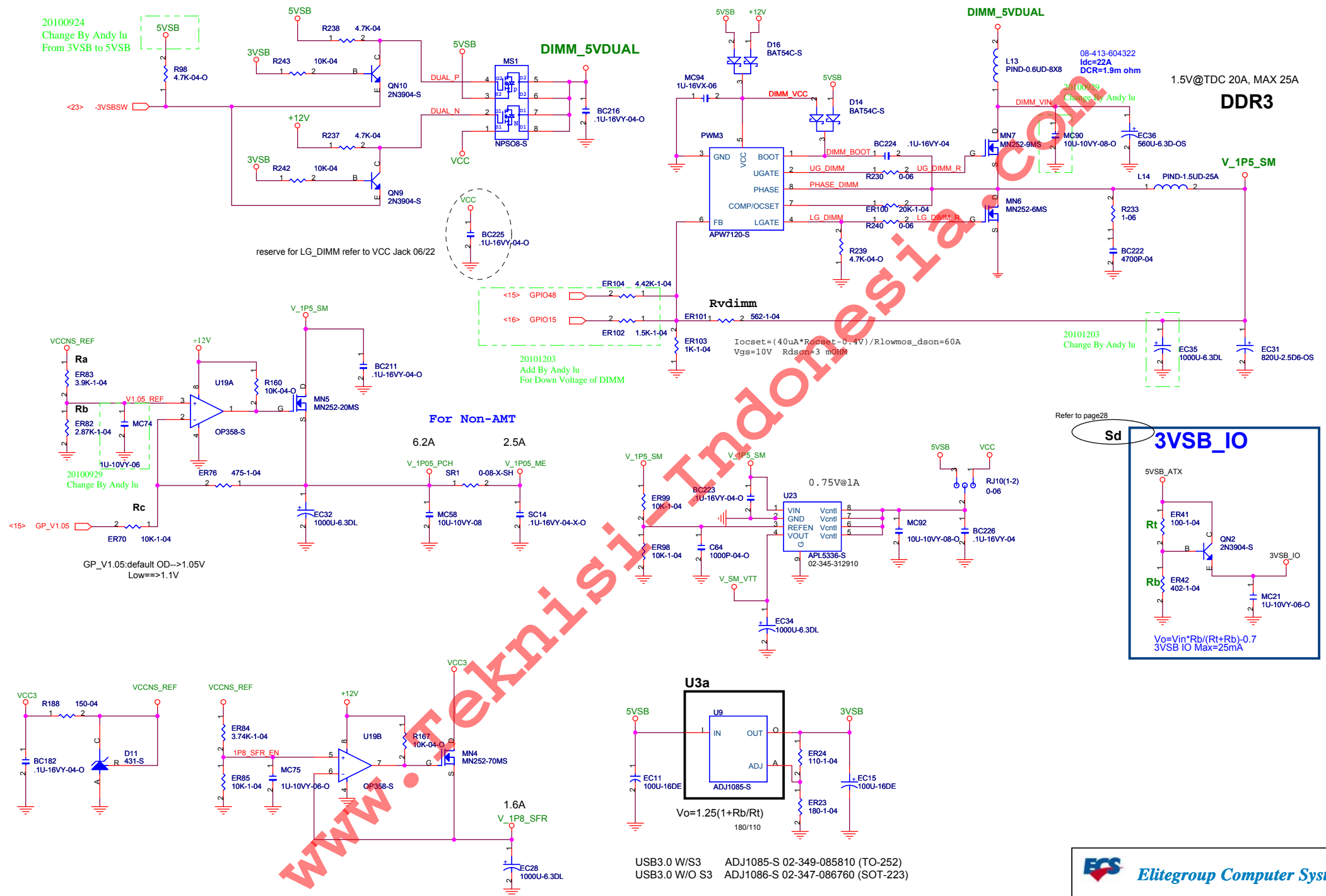
- Top line: VCC (left) to VCC (right)
- Second line: 3VSB (left) to 3VSB (right)
- Third line: 5VSB (left) to 5VSB (right)
- Bottom line: V_1P05_PCH (left) to V_1P05_PCH (right)

VCCIO voltage selection	
VTT_SEL	V_CPUVTT
low	1V
high	1.05V

VCCSA voltage selection	
VID	+V_SA
0	0.925V
1	0.85V

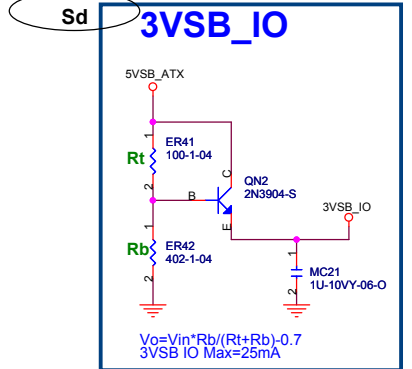


20100924
Change By Andy lu
From 3VSB to 5VSB

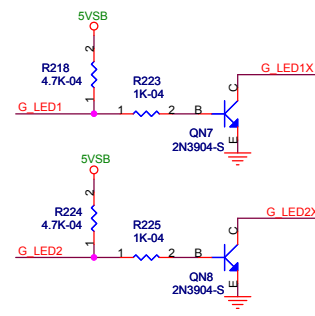
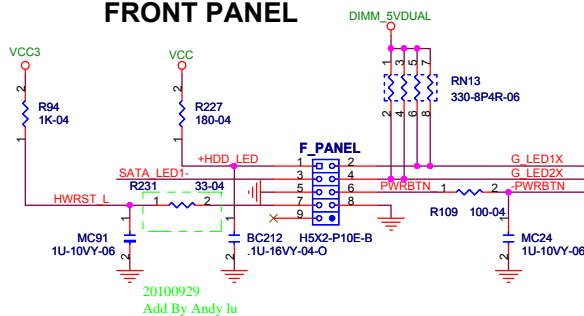
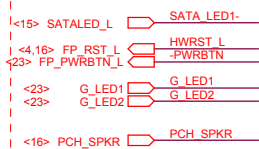


Refer to page28

Sd

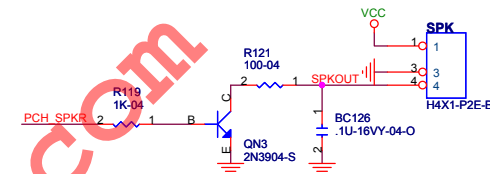


External Connection



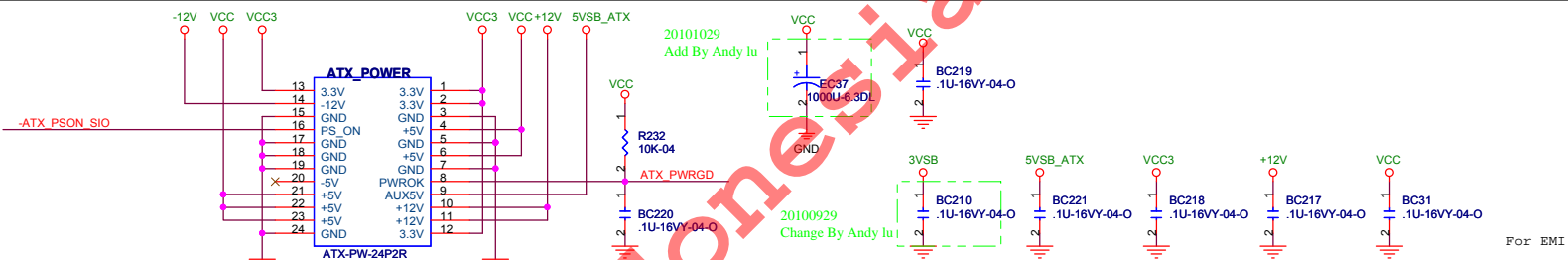
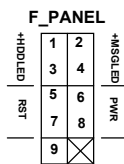
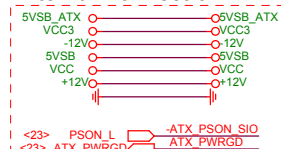
S0	S1	S3	S4	S5
G_LED1	L	B	B	L
G_LED2	H	H	L	L
G	GB	YB	OFF	OFF

B: Blinking



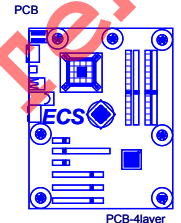
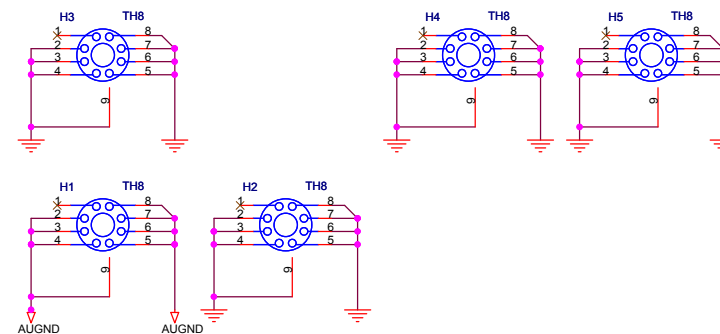
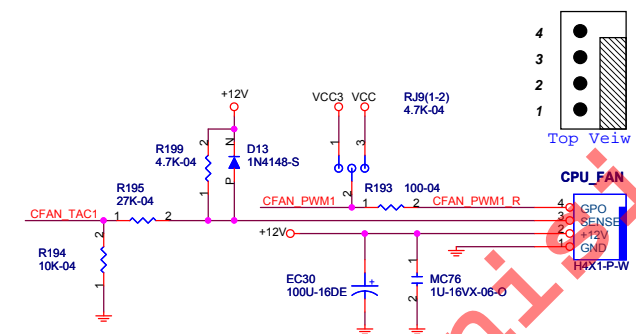
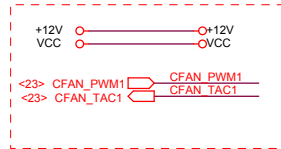
POWER CONNECTOR

External Connection



FAN

External Connection



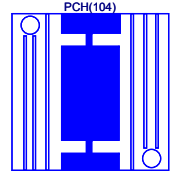
PCB STACK:

L1:TOP

L2:PWR

L3:GND

L4:BOTTOM



20-120-011476

5series PN:20-120-010851



SMD 64M

Elitegroup Computer Systems

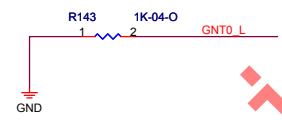
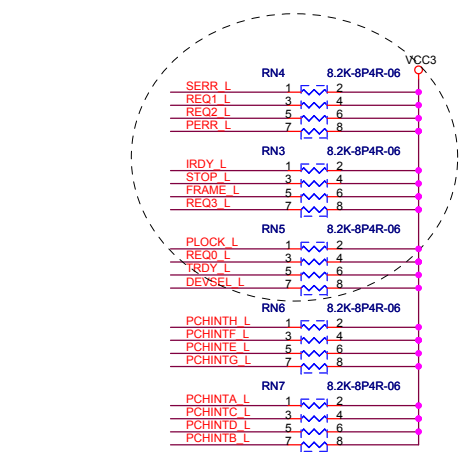
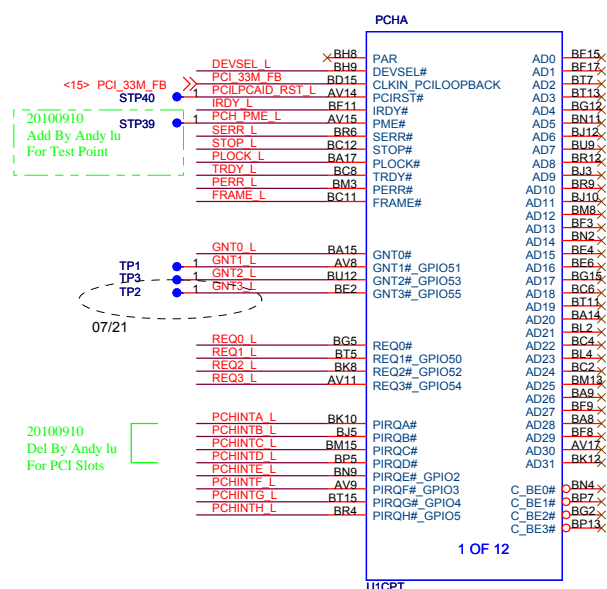
Title: Front Panel,FAN,PowerConn,GND,104

Size: Document Number: H61H2-M2

Custom: Rev: 1.0

Date: Thursday, December 09, 2010 Sheet: 13 of 29

For H61:USB Port 6/7/12/13 is disabled....From 440377 file



GPIO19:
Boot Device Select Strap.

GNT0 L:
No More Information in EDS V0.7

GNT1 L:
Boot Device Select Strap.

GNT2 L:
ESI Strap (Server Only),
DONT Pull Low in Desktop.

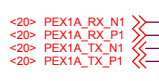
GNT3 L:
Top-Block Swap Override Mode,
When Sampled Low.

GNT[0..3]#
GPIO19
have been internal pull high to +VCC3

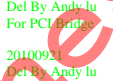
Boot Device Select:

BOOT DEVICE	GNT1_L	GPIO19
LPC	0	0
PCI	1	0
SPI	1	1

PCIEx1_A



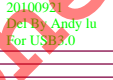
PCI bridge



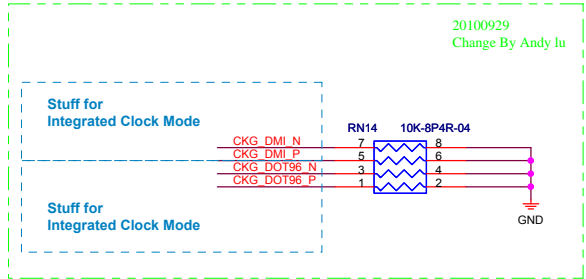
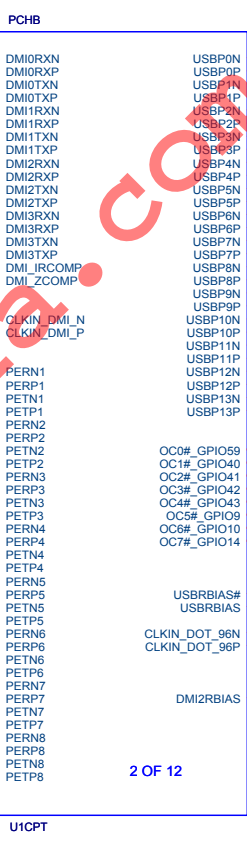
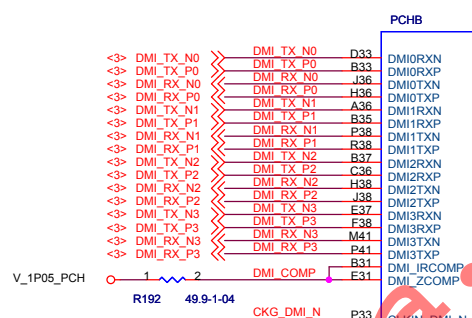
LAN



USB3.0



For H61:PCIE 7/8 is disable....From intel Jasmine

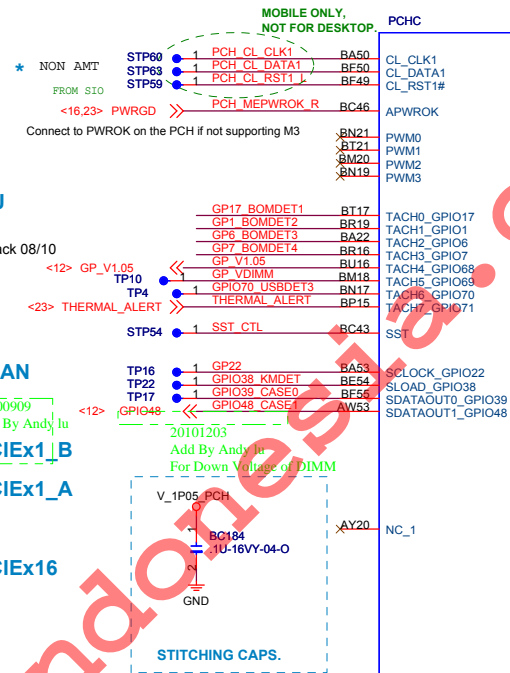


Elitegroup Computer Systems

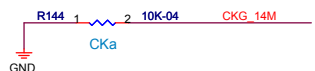
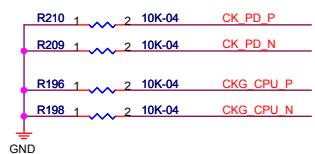
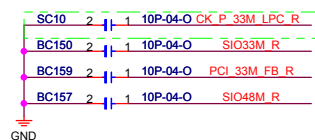
Title: **PCH - DMI/PCI/PE/USB**

Size Custom: Document Number **H61H2-M2** Rev **1.0**

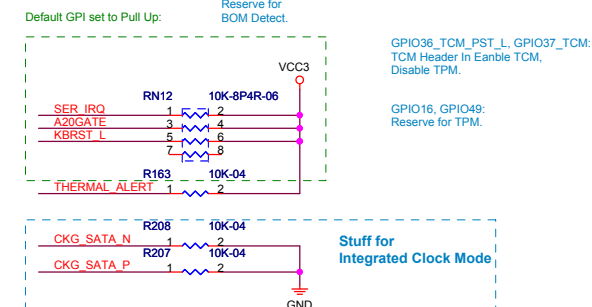
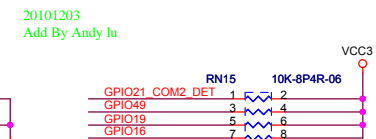
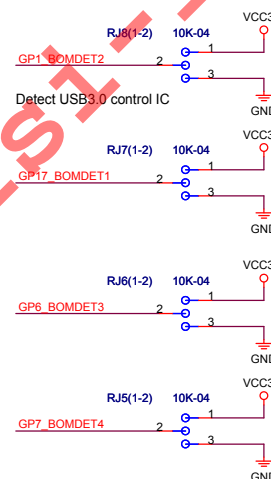
Date: Monday, December 06, 2010 Sheet 14 of 29

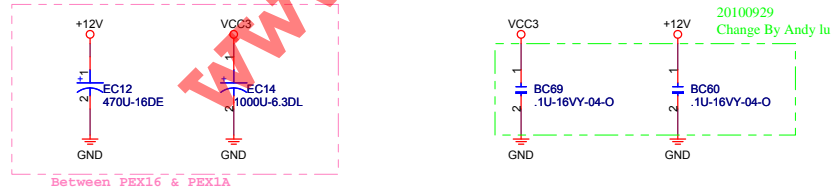
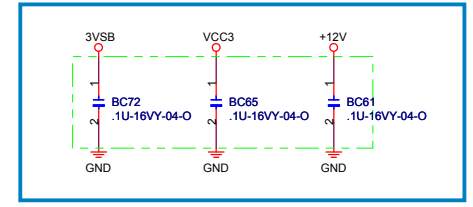
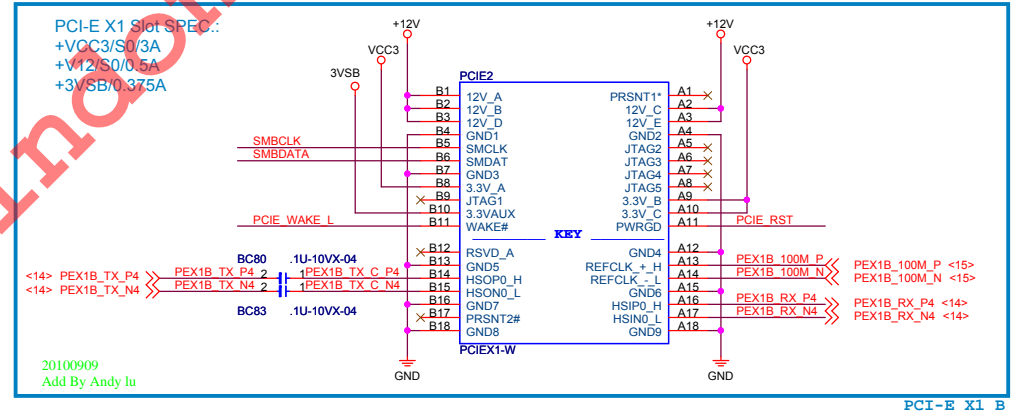
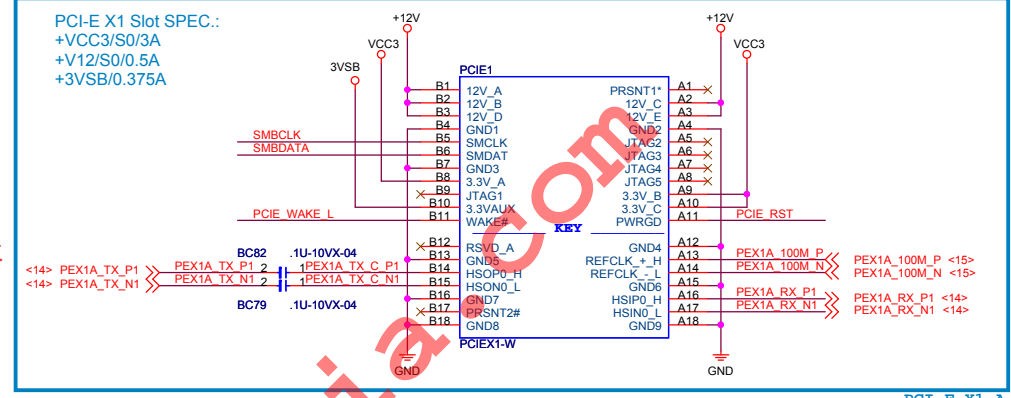
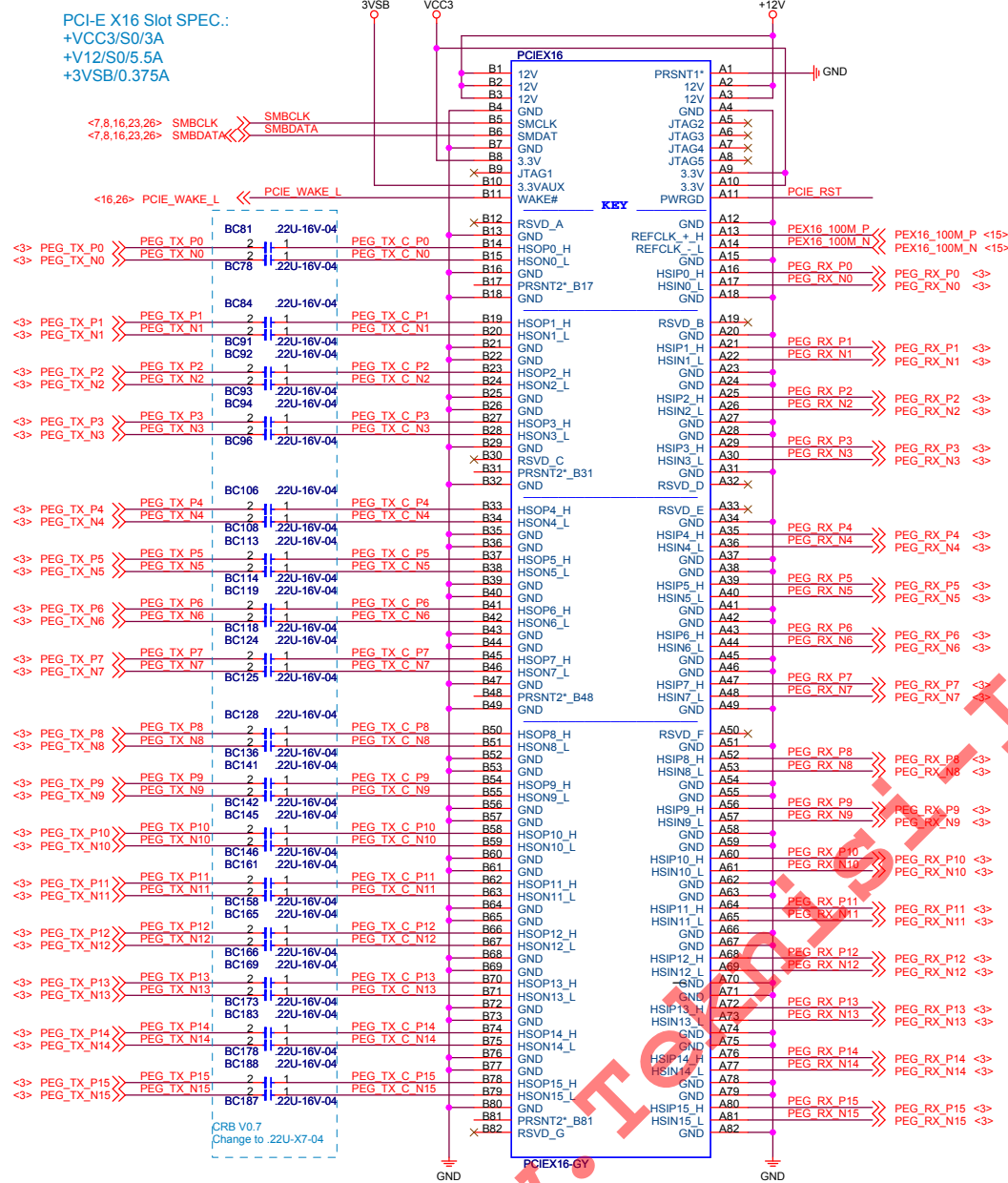


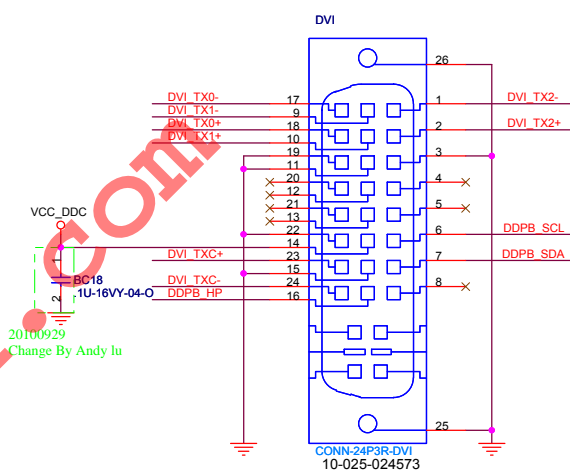
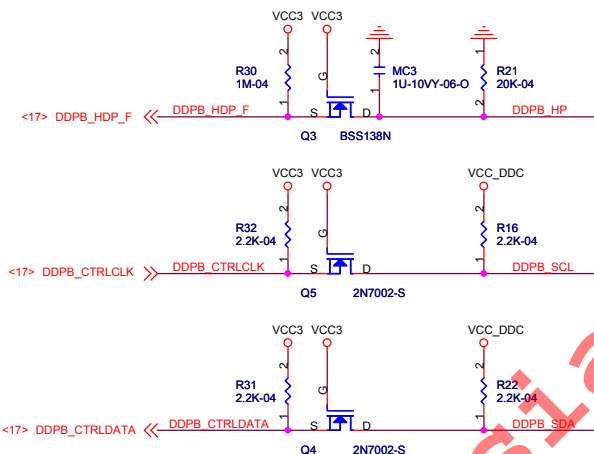
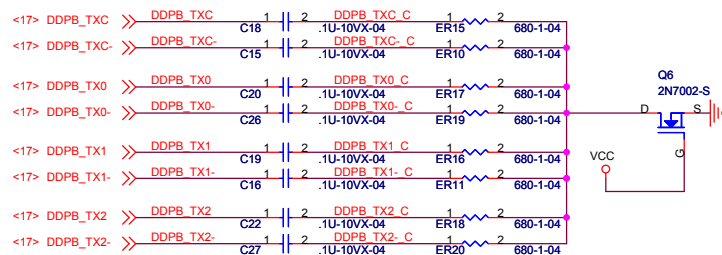
20100916
Change By Andy lu
From Ports 2,3 to Ports0,1



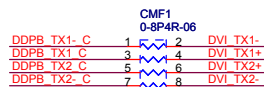
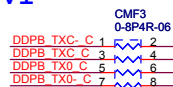
Stuff for
Integrated Clock Mode



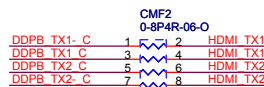
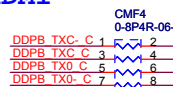




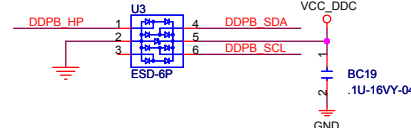
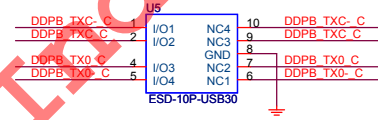
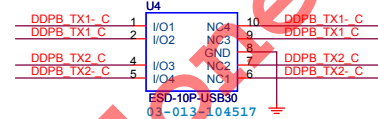
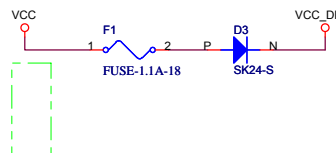
DVI



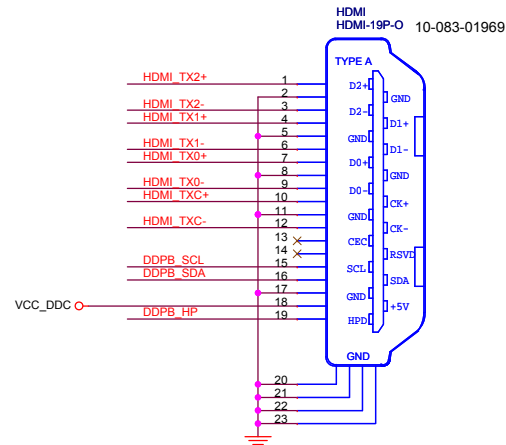
HDMI



20100928
Del MC 10UF
By Andy lu

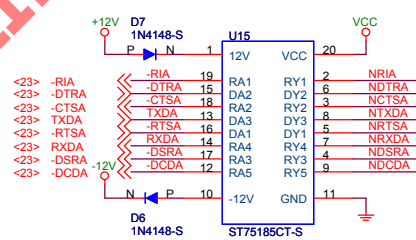
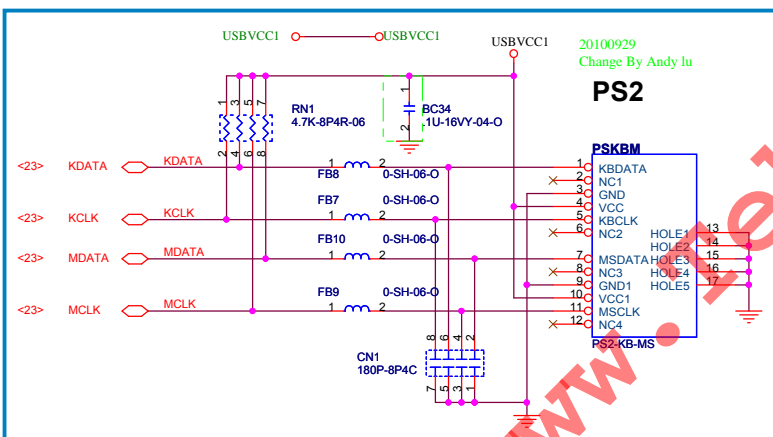


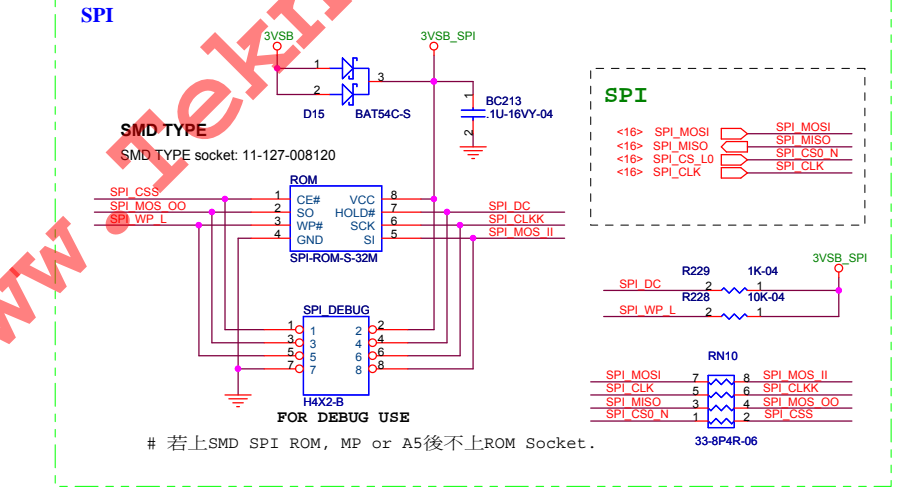
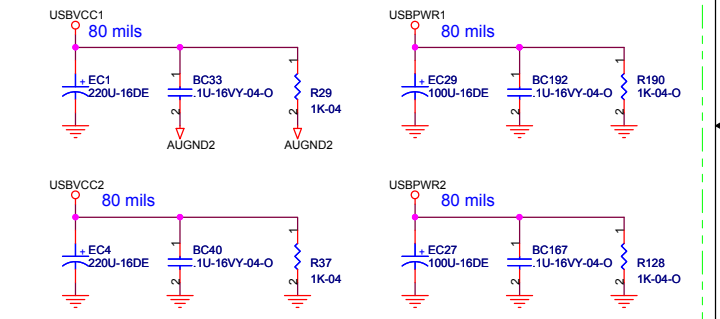
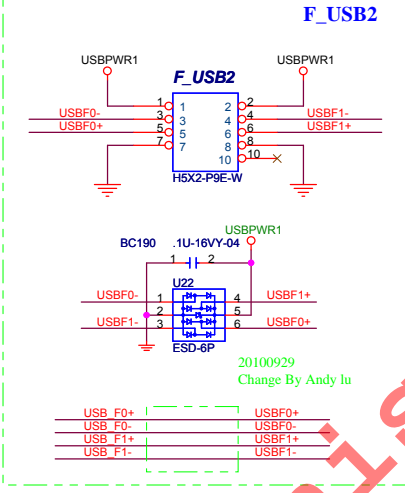
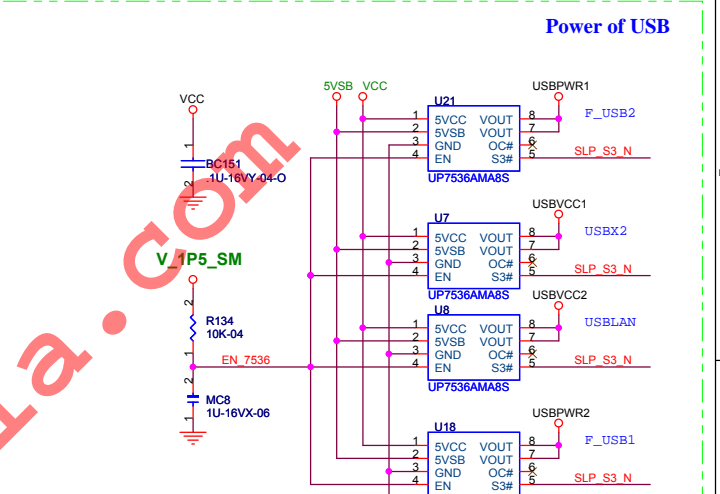
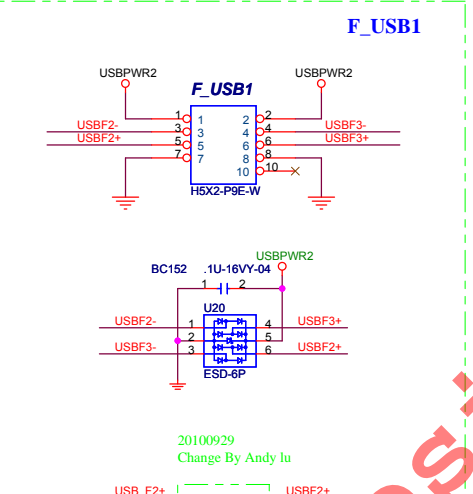
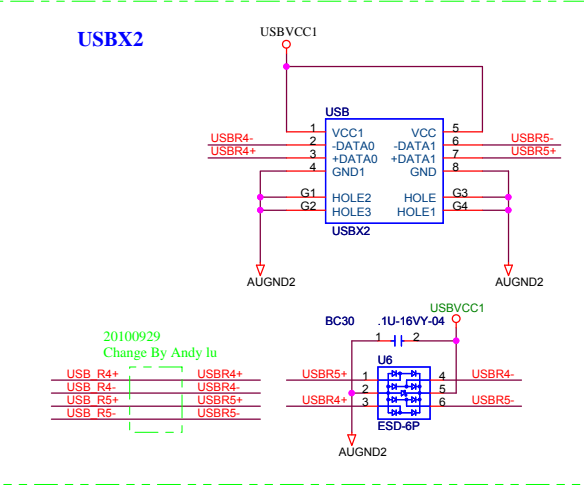
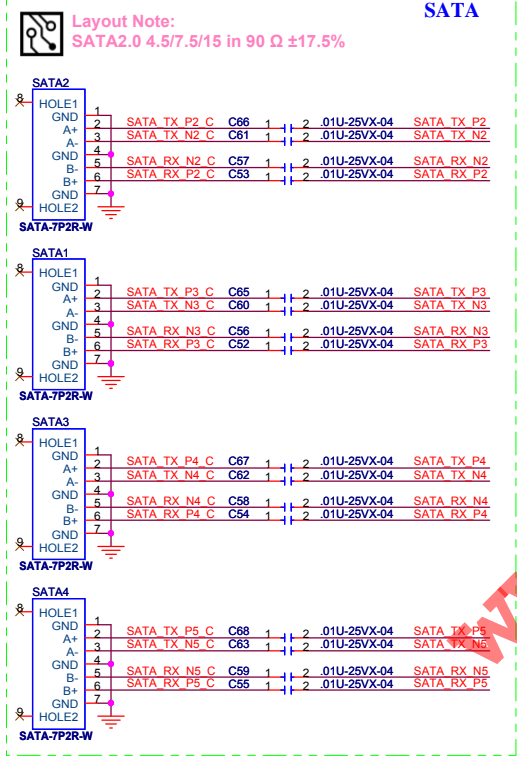
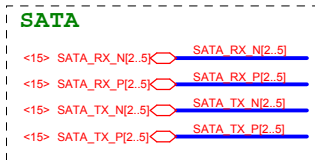
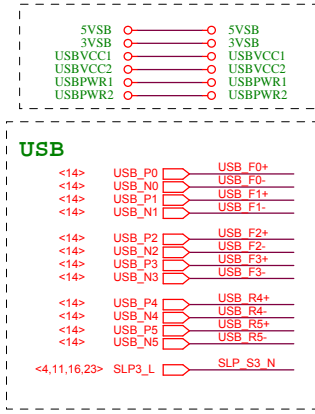
ESD



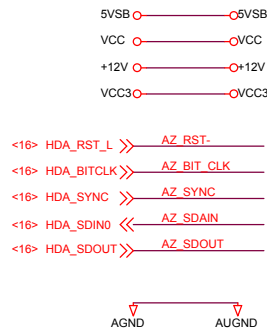
PS2

20100929
Change By Andy lu

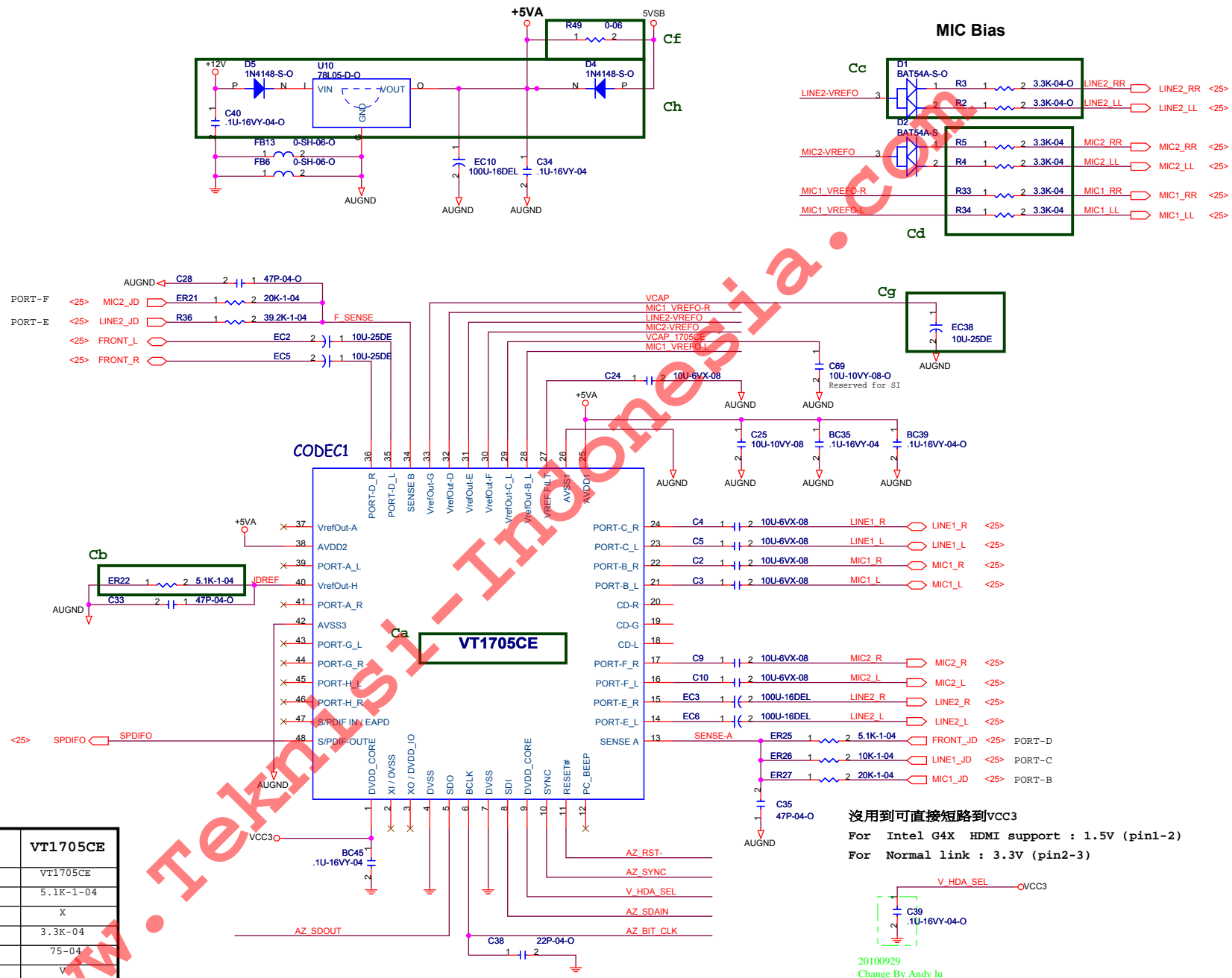




External Connection



* VCC1.5 can remove for non-Intel G4X platform

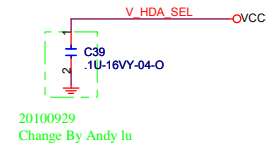


BOM Difference

Location	ALC662	VT1705	VT1705CE
Ca	ALC662-VC-GRS	VT1705	VT1705CE
Cb	20K-1-04	5.1K-1-04	5.1K-1-04
Cc	V	X	X
Cd	2.2K-04	3.3K-04	3.3K-04
Ce	75-04	75-04	75-04
Cf	X	X	V
Cg	X	X	V
Ch	V	V	X

When you change BOM, remember change GPI to inform BIOS use different Verb-Table.

沒用到可直接短路到VCC3
For Intel G4X HDMI support : 1.5V (pin1-2)
For Normal link : 3.3V (pin2-3)

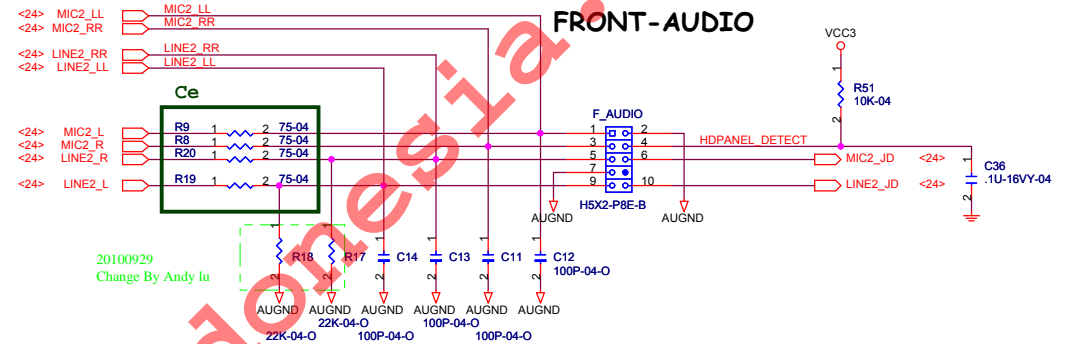
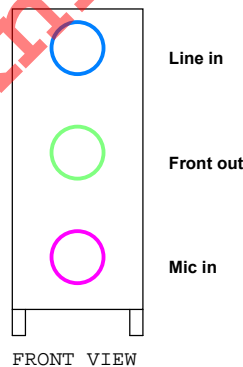
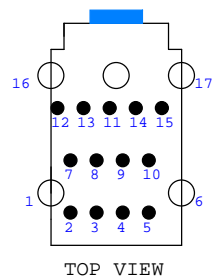
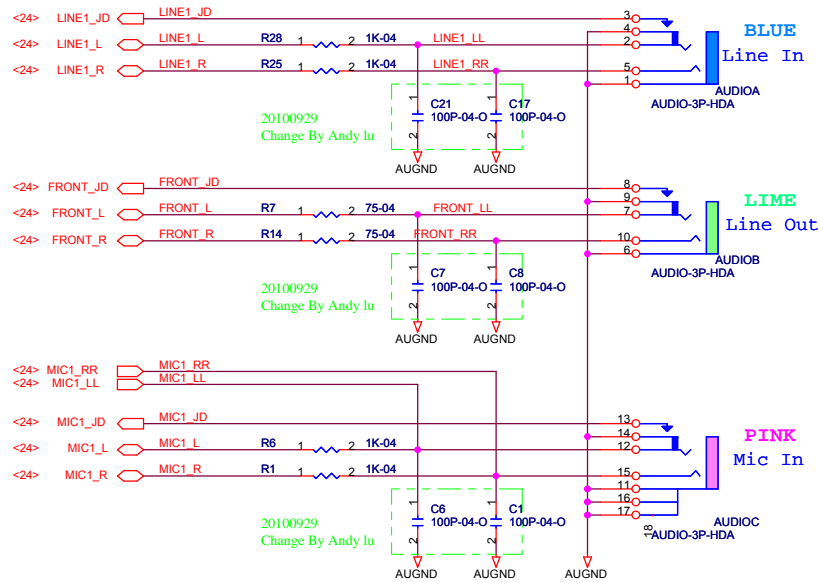


External Connection

<16> FP_AUD_DETECT << HDPANEL_DETECT

* HDPANEL_DETECT connect to SIO or SB GPIO for AC97 Panel support

REAR-AUDIO Non re-tasking for rear panel



SPDIF-OUT

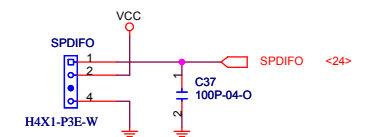
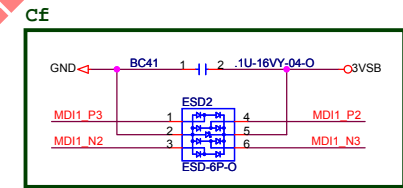
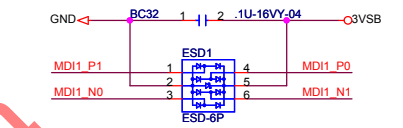
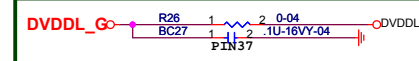
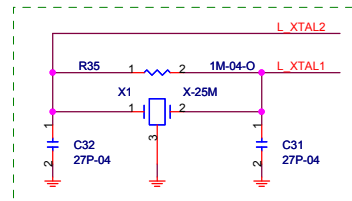
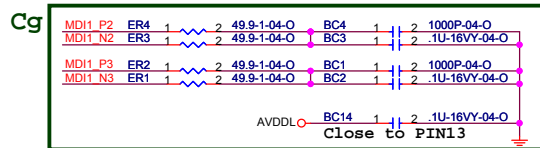
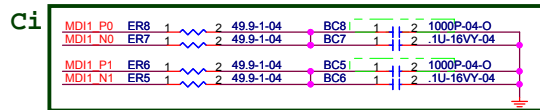
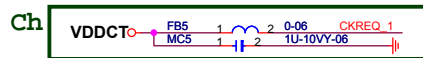
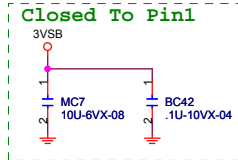
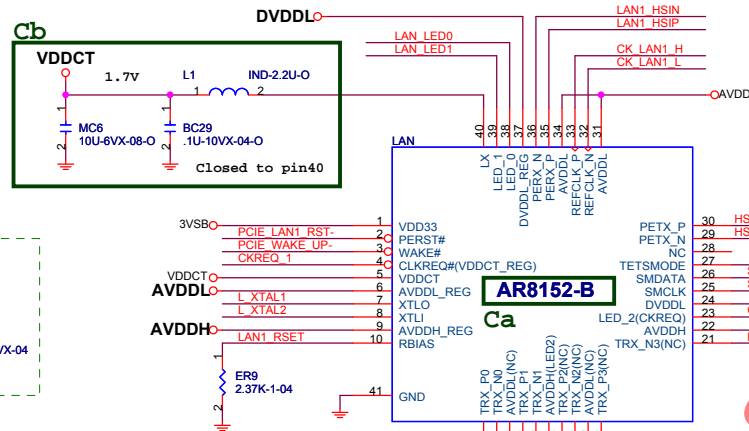


Diagram showing connections for the USB VCC2, 3VSB, VCC3, and AUGND2 pins. The connections are as follows:

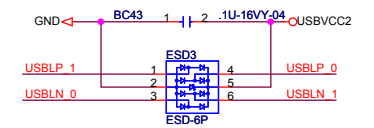
Pin	Connection
USB VCC2	USB VCC2
3VSB	3VSB
VCC3	VCC3
AUGND2	AUGND2

Pin	Connection
<16,20> PCIE_WAKE_L	PCIE_WAKE_UP
<20,23> SIO_PCIE_RST_L	PCIE_LAN1_RST
<1> CK_PE_100M_LAN_H	CK_LAN1_H
<1> CK_PE_100M_LAN_L	CK_LAN1_L
<14> LAN_TX_P6	LAN1_HSIP
<14> LAN_TX_N6	LAN1_HSN
<14> LAN_RX_P6	LAN1_HSOP
<14> LAN_RX_N6	LAN1_HSON
<14> USB_N10	USB_LN0
<14> USB_P10	USB_LP0
<14> USB_N11	USB_LN1
<14> USB_P11	USB_LP1
<8,16,20,23> SMCLK	SMCLK
<8,16,20,23> SMCDATA	SMCDATA

LAN_HSIP/N在SB的PCIE TX端要記得放AC coupling cap



USB LP0	USBLP_0
USB LN0	USBLN_0
USB LP1	USBLP_1
USB LN1	USBLN_1



	AR8151-B 1000M	AR8152-B 10/100M	AR8161-B 1000M
Ca	AR8151-B	AR8152-B	AR8161-B
Cb	V	X	X
Cc	USBX2-LAN-1000	USBX2-LAN-100	USBX2-LAN-1000
Cd	X	V	X
Ce	0-04	.01U-25VX-04	0-04
Cf	V	X	V
Cg	V	X	X
Ch	X	V	X
Ci	V	V	X
Cj	V	X	V
Ck	V	X	X
Cl	X	X	V
Cm	V	V	X
Cn	V	V	X

1 LAN_LED0 R42 1 2 330-04 ACTIVE Y

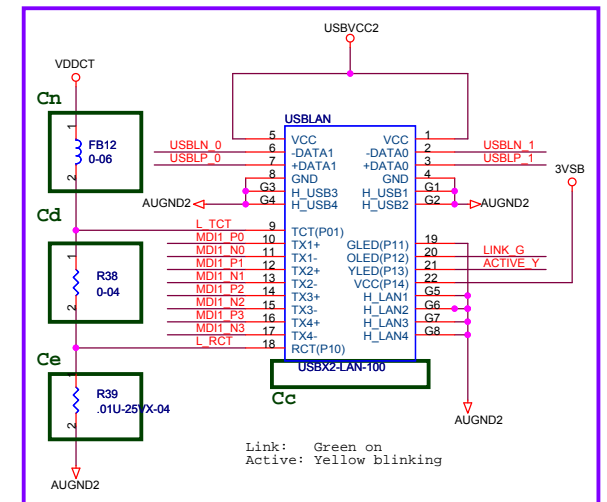
0 LAN_LED1 R40 1 2 330-04 LINK G

R41 1 2 5.1K-04

Signal	Pin	Function	Pin
DVDDL	BC38	1	2..10VX-04 PIN24
AVDDL	BC36	1	2..10VX-04 PIN34
AVDDL	BC37	1	2..10VX-04 PIN31
AVDDH	BC20	1	2..10VX-04 PIN22
VDDCT	BC28	1	2..10VX-04 PIN5

AVDDL MC4 1 2 1U-10VY-06 PIN6

AVDDH MC1 1 2 1U-10VY-06 PIN9



Link: Green on
Active: Yellow blinking

ATX P/S WITH 1A STBY CURRENT				
5VSB	5V	3.3V	12V	-12V
+/-5%	+/-5%	+/-5%	+/-5%	+/-5%

ATX4P
12V
+/-5%

Switching RT8859A 4 phases

Switching RT8121 1 phase

DDR3 DIMM (4) 1333MHz	
VDDQ	15A_S0
V_SM_VTT	1.0A_S3
V_SM_VTT	1.0A_S0

Linear OP358

LDO APL5336

Linear OP358

Linear LM324

Intel Sandy Bridge CPU		
VCCP	VDD 0.25~1.52V	85A(95W)
VAXG	VDD 0.25~1.52V	25A
VTT	1.05V(1V)	8.5A
VCC_SA	0.925V(0.85V)	8.8A
VCCPLL	1.8V	1A
VDDQ	1.5V	4.5A

Intel Cougar Point (TDP 5.5W)		
V_PROC_IO	1.05V	1mA
VccDMI	1.05V	0.057A
VccCORE	1.05V	1.6A
VccIO	1.05V	4.07A
VccADPLL	1.05V	0.1A
VccADPLLB	1.05V	0.1A
VccCLKDMI	1.05V	0.02A
VccSSC	1.05V	0.105A
VccDIFFCLKN	1.05V	0.055A
VccASW(ME)	1.05V	1.61A
VccDFTERM	1.8V	0.2A
VccVRM	1.8V	0.159A
Vcc3_3	3.3V	0.409A
VccADAC	3.3V	0.068A
VccSPI	3.3V	0.02A
VccDSW3_3	3.3V	0.003A
VccSUS3_3	3.3V	0.097A
VccSUS3_3	3.3V	0.01A
VccRTC	3.3V	6uA(G3)
V5REF	5V	1mA
V5REF_SUS	5V	1mA

NEC_D720200		
VDD3P3	3.3V	TBD
VDD1P05	1V	TBD
CTRL1P0 internal LVR Output		

SUPER I/O IT8721		
3VSB	3.3V	TBD
VCC3	3.3V	TBD
BAT 3.3V	3.3V	TBD

AUDIO ALC892		
DVDD 3.3V	3.3V	23mA
AVDD	5V	38mA

Fans
12V_200mA

SPI
VCC3_30mA

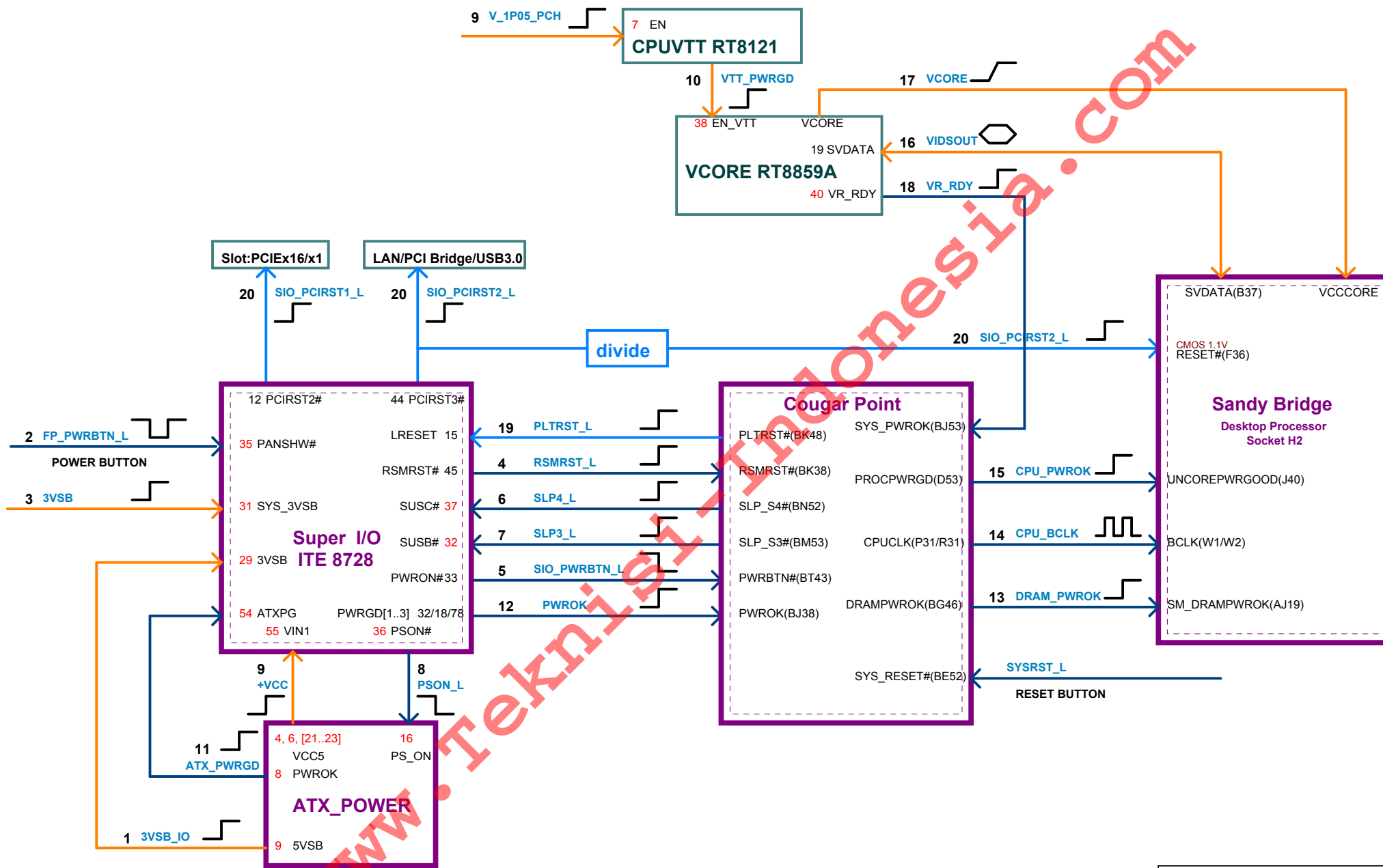
CRT
VCC_1A fuse

HDMI/DP
VCC3_0.5A fuse x 2

HDMI L.S.
VCC3_180mA

Flash/NVM
VCC3_0.3A
1.8V_0.1A

Battery 3V



NOTE:

Sugar Bay Platform has two clock mode:

1.Integrated Clock Mode (Generate by PCH)

2.Buffer Through Mode (Generate by Clock Gen.)

If we choose Integrated Clock Mode, we should unstuff Clock Gen. circuit.

Please refer to

Page.12 PCH - DMI/PCI/PE/USB for CLK IN PD

Page.13 PCH - SATA, SATA CONN for CLK IN PD

Page.14 PCH - MISC, F/W Strap

Page.15 PCH - CLK IO, CKG - CV184 for Option

